ENHANCING PHASE-MARGIN OF OTA USING SELF-BIASING CASCODE CURRENT MIRROR

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ABSTRACT

In this paper, a new adaptive biased low voltage cascode current mirror with high input/output swing is presented. This advantage is achieved using a self-biasing transistor and compensation resistor. The new structure profits from better input dynamic range and lower supply voltage without frequency response limitation and increasing input impedance. Also, the proposed current mirror is incorporated in folded cascode amplifier in order to enhance its phase-margin. The simulation results in 0.18 μm CMOS technology confirm the theoretical analysis and exhibits 478 μA linear input/output current swing and a phase-margin enhancement of 12° for the proposed current mirror and amplifier compared to the conventional circuits, respectively.

KEYWORDS

Swing, Current mirror, Dynamic range, Folded cascode, Phase-margin, Self-biasing.

1. INTRODUCTION

The demand for low power circuits is increased in last decades. The portable devices are the main purpose of these circuits due to limited power supply availability. The current mirror (CM) is one of the main parts of the most analogue and mixed-signal integrated circuits such as OTAs, current conveyers and current sensors. The low voltage cascode current mirror (CCM) has high swing and small input voltage compared to the conventional CCM. These properties make it ideal for VLSI test circuits and portable devices [1]. A low voltage CCM is shown in Fig. 1. The bias voltage V_b should be set according to the input current I_{in} in order to ensure saturation operation of all transistors. By increasing input current the operation of transistor M1 may be changed into triode region. This limitation is imposed by fixed bias voltage V_b which can't increase proportionally with input current [2]. Recent works on the CM include biasing resistor [3], linear-region transistor [3] and level shifter transistor [4] to increase input dynamic range and introduce bias voltage V_b of the low voltage CCM. But these topologies lead to the higher input voltage requirement, increasing input impedance and silicon area compared to the conventional CM. For example, a self-biasing low voltage CCM can be used in the operational transconductance amplifiers (OTAs) as the transconductance conveyer structure [5]. But this configuration leads to the phase-margin (PM) degeneration due to the larger parasitic capacitances of the self-biasing topology [6]. Therefore, the high speed CM can be introduced to compensate of such phase-margin degeneration [7, 8].

In this paper, a new self-biasing CCM with frequency compensation technique is introduced. It can operate well in low supply voltage and it has high input/output dynamic range. Also, it can be used in folded cascode (FC) amplifier in order to phase margin enhancement. The paper is organized as follow: Section 2 introduces proposed CCM with a brief comparison to the recent

works. In the next section, the enhanced phase-margin single ended FC amplifier is described. The simulation results are discussed in Section 4 followed by a conclusion in Section 5.

Figure 1. Conventional low voltage cascode current mirror.

2. PROPOSED CURRENT MIRROR (PCM)

As shown in Fig. 2a, a resistor in series with input node can be used to produce bias voltage of M1 and M3 [3]. Despite the simplicity and increased input current range of this architecture, the integrated resistor suffers from process variation, so the voltage of the gate terminals will not be precise. In addition, the value of the resistor should be decreased as input current rise further. Another architecture of the pervious circuit is shown in Fig. 2b. A linear-region MOS transistor as resistor is used in this structure which its gate is connected to the input and value of the resistor can be changed by input current [3]. Although the problems of current mirror in Fig. 2a are diminished, but minimum input voltage is approximately twice the value needed in the conventional low voltage CCM. Thus, architecture of Fig. 2b is not suitable for low voltage circuits. In addition, the input resistor of CM is increased which is not desirable for CCM. A level shifted current mirror can be used in conventional low voltage CCM for another approach [4]. As shown in Fig. 2c, when I_{in} increases (V_{in} increases too), the transistor M5 shifts the voltage level at the gate terminal of M3. As a result, input current can be increased more than conventional CM. Therefore, the problems of current mirrors in Figs. 2a and 2b are eliminated, but the chip area of current mirror in Fig. 2c is more than its counterparts. This area arises from the large size of transistor M5 and an additional bias current source. The transistor M5 should operate in sub-threshold region to achieve proper performance, so I_{bias} should be small enough to keep M5 at this region and consequently the aspect ratio of transistor M5 should be large [4].

Figure 2. Cascode current mirrors with adaptive biasing: (a) resistor biasing of cascode transistors, (b) linear-region transistor biasing of cascode transistors, and (c) level shifted current mirror.

The proposed CM is illustrated in Fig. 3. In this circuit, PMOS transistor M5 creates a bias voltage for cascode transistors M3 and M4 of current mirror. The body effect is removed by connecting the body to the source terminal of M5 for decreasing the input voltage requirement. To ensure saturation operation of M1 and M3, the input voltage V_{in} should be

$$V_{in} = V_{SG5} + V_{ov1} = V_{th} + V_{ov3} + V_{ov1} \quad (1)$$

where V_{ov1} and V_{ov3} are overdrive voltage of transistors M1 and M3 which are founded by (2) and (3), respectively.

$$V_{ov1} = \sqrt{\frac{2I_{in}}{K'A_1}} \quad (2)$$

$$V_{ov3} = \sqrt{\frac{2I_{in}}{K'A_3}} \quad (3)$$

where $A_1=W_1/L_1$, $A_3=W_3/L_3$ and W_j , L_j are width and length of transistor M_j, respectively.

Figure 3. Proposed low voltage cascode current mirror.

The body effect is ignored and it is assumed that all transistors have the identical threshold voltage V_{th} and transconductance parameter $K=C_{ox}\mu$. The input voltage and input current can be found by replacing equations (2) and (3) in (1).

$$V_{in} = V_{th} + 2V_{od} = V_{th} + \sqrt{\left(\frac{2I_{in}}{K'}\right)\left(\frac{1}{A_1} + \frac{1}{A_3}\right)} \quad (4)$$

$$I_{in,min} = \frac{K'(V_{in} - V_{th})^2}{2\left(\frac{1}{\sqrt{A_1}} + \frac{1}{\sqrt{A_3}}\right)^2} \quad (5)$$

From the above equations, it can be seen there is a relation between input voltage V_{in} and input current I_{in} that leads to the self-biasing CCM configuration and a large upper limit. Because all input current/voltage changes will transfer to the cascode transistors through M5. Therefore not only the circuit has a very large upper input current limit ($I_{in,max}$) but also it has very small value of current gain error rate ($I_{out}-I_{in}=0$) compared to the conventional CMs. Transistor M5 leads to

bandwidth degeneration of CCM due to new added parasitic capacitances. But this problem can be resolved by compensation resistor [7, 8]. As shown in Fig. 4 by adding a transistor M6 in deep triode operation region, the new transfer function of circuit can be written by

$$H(s) = \frac{\frac{gm_1}{c_3} \left(S + \frac{1}{R_6 c_1} \right) \left(S + \frac{gm_3}{c'} \right)}{S^3 + S^2 \left(\frac{R_6 c_1 k gm_3 + c' (k+1)}{R_6 c' c_1 k} \right) + S \left(\frac{gm_3 (k^2 c_3 + k c') + k gm_5 c_3}{R_6 c' c_1 c_3 k^2} \right) + \frac{gm_3 gm_5}{R_6 c' c' c_3 k}} \quad (6)$$

Where k is the current gain ($k = I_{out}/I_{in}$), $kC_1 = C_{gs2} = kC_{gs1}$, $kC_3 = kC_{gs3} = C_{gs4}$ and $C' = C_{gs3} + C_{gs5}$ are the gate-source capacitances, and $gm_2 = k gm_1$, $gm_4 = k gm_3$ and gm_5 are the transconductance of each transistor and R_6 is the resistor value of the M6. The transistor M6 generates a pole-zero pair to the transfer function and does not consume power due to the deep triode operation region. The new transfer function has 2 zeroes and 3 poles. By increasing the value of R_6 , the new added pole-zero pair move from negative infinity toward the origin of the axes. The maximum bandwidth occurs when the zero cancels the low-frequency pole. In this condition, the value of R_6 can be obtained by

$$R_6 = \frac{c' (k+1)}{k gm_3 (c_{gs1} + c_{gd6})} \approx \frac{c' (k+1)}{k gm_3 (c_{gs1})} \quad (7)$$

Figure 4. Proposed low voltage cascode current mirror with frequency compensation.

Furthermore, the input impedance is approximately as low as conventional CCM due to the feedback path from gate of M5 to the drain of M1 [9]. The input impedance can be calculated by

$$R_{in} = \frac{1}{gm_1} \left[1 + gm_1 r_{o5} \frac{r_{o5} (gm_3 - gm_5)}{gm_5 r_{o5} + gm_3 r_{o3}} \right] \quad (8)$$

By assuming $gm_3 = gm_5$, (8) can be simplified to

$$R_{in} = \frac{1}{gm_1} \quad (9)$$

3. ENHANCED PHASE-MARGIN FOLDED CASCODE AMPLIFIER

The conventional single ended folded cascode (FC) amplifier in [5] has two prominent poles ω_{p1} , ω_{p2} which are obtained by (10) and (11), respectively.

$$\omega_{p1} = -\frac{1}{R_{out}C_{load}} \quad (10)$$

$$\omega_{p2} = -\frac{gm_1}{2C_{gs1}} \quad (11)$$

Also, it has a zero at $\omega_{z1}=2\omega_{p2}$ [5, 6]. In order to have a good phase-margin, ω_{p2} can be chosen $\omega_{p2} \geq 3\omega_u$, where ω_u is unity gain frequency of amplifier. By placing proposed low voltage CCM in folded nodes of the conventional FC topology which is described in [6], the new structure with proposed CCM is shown in Fig. 5.

In this amplifier, the non-dominant pole moves further away from the origin and a new zero added which can be chosen such that cancel the transposed pole. The transfer function of current mirror from ground node to folded node (node X) becomes (M3, M4 excluded)

$$H(s) = \frac{I_2(s)}{I_1(s)} = \frac{gm_2 \left[S + \left(1/R_6 C_{gs1} \right) \right]}{C_{gs1} S^2 + (2/R_6) S + (gm_1/R_6 C_{gs1})} \quad (12)$$

Figure 5. The proposed enhanced phase-margin folded cascode amplifier.

The new pole and zero are described by (13) and (14), respectively.

$$\omega'_{p2} = -\frac{gm_1}{C_{gs1}} \quad (13)$$

$$\omega_{z2} = -\frac{1}{R_6 C_{gs1}} \quad (14)$$

By choosing $R_6 = 1/gm_1$, ω_{z2} will be equal to ω'_{p2} , thus the zero cancels the first non-dominant pole of the proposed amplifier and the new first non-dominant pole is determined by parasitic capacitor at folded node. Thus, the phase-margin of the proposed amplifier can be enhanced. Also, the high-speed CCM does not introduce additional poles and zeros. Therefore, the GBW of the proposed amplifier is not limited, which is some enhanced compared to that of the conventional FC.

4. SIMULATION RESULTS

The proposed current mirror (PCM) and proposed folded cascode (PFC) amplifier are simulated in 0.18 μ m CMOS technology with power supply voltage of 1.8 V. The current gain error rate ($I_{out}-I_{in}$) and the tolerable input voltage range of the proposed CM with comparison to the conventional CM is shown in Figs. 6a and 6b, respectively. The maximum current gain error rate of the proposed CM is 1.6% in the input current range of 12 μ A to 490 μ A. Also in this range, the input voltage changes from 575 mV to 1.6 V. It is evident that both current error and input dynamic range are significantly improved. Namely, in the wide range of the input current/voltage variations, all transistors of the proposed CM will remain in the saturation region of the strong inversion to have a linear operation.

Figure 6. (a) The current gain error rate for proposed and conventional CMs, and (b) the Input voltage variations with respect to the input current for proposed and conventional CMs.

The frequency response of the proposed and conventional amplifiers is presented in Fig. 7a. This figure shows 222MHz bandwidth improvement of the proposed CM compared to the conventional CM. Also, the frequency response of the amplifiers is shown in Fig. 7b. For design of amplifiers, both the FC and PFC are loaded with 2.5 pF capacitor. The size of transistor M6 is adjusted to cancel the first non-dominant pole and the phase-margin enhancement. It can be seen that the phase-margin is improved by 12°. Furthermore, the GBW is increased by 22.4 MHz without sacrificing any performance.

Figure 7. (a) Frequency response of the proposed and conventional FC amplifiers, and (b) frequency response of the compensated and conventional CMs.

Figure 8. (a) Temperature variations of the proposed CM, and (b) corner analysis of the proposed FC amplifier.

The designed proposed circuits demonstrate relatively suitable response in different temperatures and process corners. Figs. 8a and 8b show the effects of temperature dependent on output current of the proposed CM and corner processes on frequency response of the proposed FC, respectively. As shown, in FF corner, the bandwidth of the PFC is increased by 4% and the phase-margin by 2.8° while the DC gain decreased by about 9 dB. In SS corner, the bandwidth of the PFC is decreased by 3.5 %, the phase-margin by approximately 2.3° and DC gain by 3.5 dB. Table 1 summarizes the specifications of the PCM, PFC and recent works. Also, table 2 details the transistor sizes used in the simulation of the PCM and PFC circuits. To evaluate these works two figure of merits (FOM) for amplifiers and current mirrors can be defined by (15) and (16), respectively.

$$FOM_{OTA} = \frac{(DC \text{ gain})(Unit \text{ gain frequency})(P.M.)}{(Power \text{ dissipation})} \quad (15)$$

$$FOM_{CM} = \frac{(Input \text{ current swing})}{(Maximum \text{ current gain error rate})(Minimum \text{ input voltage})} \quad (16)$$

Table 1. Specifications of the PCM and PFC in comparison with conventional circuits and to recent works.

FC amplifiers			Current mirrors				
Specifications	FC	PFC	Specifications	CM	PCM	[3]	[3]
Supply voltage (V)	1.8	1.8	Supply voltage (V)	1.8	1.8	1.8	1.8
GBW (MHz)	63.7	86.1	Minimum input voltage (V)	0.35	0.575	0.9	0.575
DC gain (dB)	59	59	Minimum output voltage	0.35	0.35	0.35	0.35
Power consumption (μ W)	750	750	Input current swing (μ A)	120	478	260	180
Phase-margin (degree)	74	86	Input voltage swing (V)	0.35	1.025	0.8	1
Input voltage noise @ 1kHz (nV/sqHz)	120	120	Maximum current gain error rate	High	1.6 %	3.1%	2.8%
Estimated area (μm^2)	5000	5000	Estimated area (μm^2)	450	500	600	600
FOM (dB.MHz.deg/ μ W)	370	582	FOM (μ A/V.%)	Low	520	93	111

Table 2. Transistor sizes (μm) of the PCM and PFC circuits.

Device	Proposed CM	Proposed FC
Mb	-	50/1
M0	-	158/1
M1, M2	30/1	30/1
M3, M4	15/1	15/1
M5	54/1	54/1
M6	14/1	14/1
M7, M8	-	86/1
M9, M10	-	81/1
M11, M12	-	171/1

3. CONCLUSIONS

A new biased cascode current mirror with high input/output swing without frequency response degeneration has been presented in this paper. By using proposed CM in folded cascode amplifier, the phase margin of the FC amplifier is improved without bandwidth limitation. Simulation results in 0.18 μm CMOS technology exhibits 478 μA linear input/output current swing of the proposed CM and a phase-margin enhancement of 12° for the proposed FC amplifier compared to the conventional circuits, respectively.

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