DESIGN AND IMPLEMENTATION OF PLL FREQUENCY SYNTHESIZER USING PE3336 IC FOR IRS APPLICATIONS

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ABSTRACT

The design and experimental verification of a low phase noise phase locked loop (PLL) frequency synthesizer using Peregrine's PE83336 IC is presented. This PLL is used as frequency synthesizer which generates stable and low phase noise signal for space applications. A stable reference frequency of 22.8MHz is provided to the PLL through a temperature compensated crystal oscillator (TCXO). Experimental results of the PLL frequency synthesizer shows the excellent performance achieved at X-band. The PLL model implemented with frequency resolution of 5.8MHz, and phase noise better than -81dBc/Hz @ 1 kHz offset at X-band. The complete model is fabricated on RT-duroid 6010 substrate.

KEYWORDS

TCXO, Phase-Locked Loop (PLL), VCO, Prescaler.

1. INTRODUCTION

Frequency synthesizer is the essential component of modern wireless communication systems and its performance will affect the quality of wireless communication systems directly. Frequency synthesizer technology is now an important part of RF development and RF equipments. Frequency synthesis is the frequency changing process whereby a new frequency is derived from a given fundamental frequency by combinations of several additions, subtractions, multiplications and divisions.

Frequency synthesizer is broadly divided into Direct and Indirect synthesizer. The Direct forms of frequency synthesizer are implemented by creating a waveform directly without any form of frequency transforming element. Direct synthesizer is further sub-divided into Direct Analogue Frequency Synthesis (DAFS) and Direct Digital Frequency Synthesis (DDFS) [1]. DAFS has excellent switching time performance, but it consumes more power as it needs to integrate mixer, filter, etc. DDFS has excellent frequency switching time, low phase noise and extremely tiny resolution, but it can't generate high output frequency, and its spurs are generally weak [2].

Indirect frequency synthesizer is based on phase locked loop technology where the output signal is generated indirectly. In other words the final signal is generated by an oscillator that is controlled by other signals. In other words the VCO output is indirectly controlled by a lower stable reference frequency in order to obtain high stable output frequency. PLL frequency

synthesizer has a wide output range as compared to all above mentioned scheme and also provides great suppression to spurious signals.

Integer N-type PLL frequency synthesis structure on RT-duroid 6010 substrate is proposed and implemented in this paper. The implemented module has excellent performance with frequency resolution of 5.8MHz, phase noise better than $-81\text{dBc/Hz}@1\text{kHz}$ at X-band. The measured result of frequency synthesizer phase noise is matched with the theoretical estimated values, as described later in this paper.

2. WORKING

2.1 Theory

By subtracting, adding, dividing or multiplying a precise and stable standard reference frequency through multiplier, mixer or divider, the synthesizer generates many combinations of the signal with the same accuracy and stability. Figure. 1 shows the block diagram of integer-N PLL. The PLL consists of a reference oscillator, frequency dividers, Voltage Controlled Oscillator (VCO), programmable divider (1/N), Phase Frequency Detector (PFD) and a loop-filter.

The reference oscillator operates at a constant frequency, while the VCO is driven by a voltage source. The VCO frequency is divided by a prescaler to bring the VCO frequency closer to stable input frequency. The divided VCO frequency is compared to the reference frequency in the PFDs. When the VCO is running slow, clock edges from the divided VCO frequency will lag the reference clock edges. The differences in phase are detected by the phase detector, and up pulses are generated, similarly when the VCO is running fast, the reference clock will lag the divided VCO frequency and down pulses will be generated accordingly. This phase difference will be detected and the charge pump will adjust the control voltage until the phase difference between the reference clock and the divided VCO clock is zero [3]. At this point, the PLL is said to be locked.

Figure 1. Block diagram of PLL frequency synthesizer using PE83336 IC.

2.2. Mechanism

The PLL compares the phase between the signal and F_c obtained by dividing the reference frequency F_r and F_p obtained by dividing the frequency of VCO by Prescaler and programmable divider and generates a error signal which is given to the VCO through a loop filter to control VCO output frequency. This continues till the loop gets looked i.e., VCO gets locked to the frequency and phase of TCXO [4-7]. The frequency resolution is obtained by the Equation (1).

$$F_c = F_r \div (R+1) \quad (1)$$

The stable reference signal (F_r) is given by TCXO. The phase detector input (F_p) is given by the Equation (2)

$$F_p = F_{in} \div [10(M+1) + A] \quad (2)$$

where A and M are the counter values. The output signal from the VCO is given to the divide by-8 prescaler which downscale it by factor 8. This output frequency F_{in} is given by obtained (3). In locked condition both Equation (1) and (2) must be satisfied.

$$F_{in} = [10(M+1)+A] \times [F_r \div (R+1)] \quad (3)$$

3. CIRCUIT DESCRIPTION

The five basic components of a PLL circuit are the phase-frequency detector, the loop filter, frequency dividers and the VCO. Typically, the PLL frequency synthesizer IC integrates the phase detectors and dividers onboard. The reason for not integrating the VCO and loop filter is to prevent the noise associated with the phase detector and digital dividers from coupling with the VCO's circuitry.

In this paper, Peregrine's PE83336 IC chip integrates the phase frequency detector and dividers (R and N). An external divide by 8 prescaler is used to downscale the VCO output frequency within the specified acceptable range of the PE83336 IC.

The described analysis in section 2 is used to realize X-band carrier generator using PLL synthesizer. The circuit realisation is described in the following parts-

3.1. Part A

Peregrine's PE83336 IC is a 44-pin, integer-N PLL chip which can synthesis up to 3.0 GHz. The IC consists of a phase detector, counters, prescaler and control logic as shown in Figure. 2. The modulus prescaler divides the VCO frequency by either 10 or 11. Counters "M" and "R" divide the F_{in} and reference frequency, respectively, by integer values stored in register. The phase frequency detector generates down and up frequency control signals [7]. Data can be written via parallel bus, series bus, or hardwired direct to the pins. The direct hardwire is chosen in our application as it provides the flexibility to avoid external processor which was required in serial or parallel bus. The circuit realization using PE83336 is shown in Figure. 3.

Figure 2. Functional block diagram of PE83336 IC.

3.2. Part B

Loop filter is broadly divided into active and passive loop filters. Active loop filter is used in this application due to its wide operating frequency range. Active loops make use of op-amps which allow the synthesizer to generate tuning voltage levels higher than that the PLL IC can generate on-chip. The necessary DC amplification is achieved using the op-amps.

Fig. 4 represents the active loop filter connected to the differential output of the PE83336 IC phase detector. The ideal values of resistor and capacitor in loop filter are obtained from the simulation carried out on system software provided from the PE83336 IC manufacturers.

3.3. Part C

A Teledyne Cougar OAS 8900 VCO with operating range of 6900 to 8900 MHz is used in this work. It offers wide tuning range, low phase noise and high frequency of operation, eliminating the need of additional frequency multipliers to obtain the desired output frequency. The VCO output is applied back to the PE83336 IC through a 10dB coupler and a prescaler (divide by 8), so that L-band frequency reaches to F_{in} pin of the PE83336 IC chip.

The circuit diagram shows a differential signal conditioning circuit. Two input signals, PD_U and PD_D, are connected to a pair of resistors (R6, R7) with a value of 120R. These resistors are connected to the non-inverting input (pin 3) of an operational amplifier (U1, OP-27). The inverting input (pin 2) is connected to a network of resistors (R1, R11) and capacitors (C18, C19). A feedback resistor (R3) with a value of 100R is connected between the output (pin 6) and the inverting input. The output signal is labeled CTRL_VOL. The circuit is powered by a +15V supply and a -15V supply. Various capacitors (C1, C2, C3, C4, C5) and resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11) are used for signal conditioning and timing. The circuit is labeled with component values and pin numbers.

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Figure 5. Circuit realization of VCO and Prescaler (block C).

4. RESULTS

The proposed frequency synthesizer consists of the PE83336 chip integrated with phase detector and programmable frequency divider, TCXO, VCO, loop filter and prescaler. The desired technical requirements of the PLL frequency synthesizer are mentioned below in Table 1.

Specification	value
Frequency Band	X-band
Phase noise	≤ -80 dBc/Hz at 1 KHz offset
Spurious	≤ -50 dBc
Harmonic suppression	≤ -30 dBc
Output Power	7 dBm (min)
reference frequency	22.8 MHz

Table 1 Desired Specification

The PLL phase noise deteriorates from the TCXO phase noise by the given equation (4)

$$PLL \text{ Phase Noise} = \text{Phase noise of TCXO} + 20 \log (F_{out}/F_r) \quad (4)$$

Figure 6. Phase noise of TCXO

The TCXO phase noise is obtained from figure 6. The PLL phase noise of -37dBc/Hz at 100 Hz is calculated from Equation (4) when F_r is taken 22.8MHz and f_{out} at X-band. This phase noise matches with the phase noise obtained practically as shown in figure (7).

The performance (phase noise) of the PLL discussed in this paper is at par with performance of the recently developed PLLs. The Comparison in terms of Phase noise reported in this paper (- 82.56 dBc/Hz @ 1 KHz at X-band) with earlier developed PLL's is given in the table below-

Publications(references)	X-Band Phase noise @ 1KHz
[1]	-71 dBc/Hz
[8]	-50 dBc/Hz
[9]	-80 dBc/Hz
[10]	-92.67 dBc/Hz
[11]	-103.96 dBc/Hz
[12]	-106 dBc/Hz

Table 2 Phase noise of recently developed PLL models.

In this application, the image can be reconstructed if the Bit Error Rate in the received data is better or equal to 1×10^6 . The phase noise of this developed PLL at X-Band seen in fig 7 is sufficient for this purpose.

Figure 7. Phase noise of PLL

The X-band carrier from PLL synthesizer is multiplied by a frequency tripler (X3) and driven through driver amplifier as per the application requirements in this work. Fig.8 and 9 shows the output spectrum of the PLL synthesizer at Ka-band(X-band multiplied by X3).

5. CONCLUSION

An analog PLL frequency synthesizer intended for carrier generation application at X and Ka-band has been presented in this paper. Design and implementation of a Low Phase Noise carrier generator using PLL synthesizer on RT-duroid 6010 substrate is implemented. An active loop filter which provides wide operating range and better filtering is used here. This implemented model shows frequency resolution of 5.8 MHz and the phase noise better than -81 dBc/Hz @ 1kHz offset.

Figure 8. PLL frequency synthesizer output at Ka-band for measuring phase noise.

Figure 9. PLL frequency synthesizer output at Ka-band showing the spectral purity

Figure 10. Top view of low noise PLL synthesiser on RT-duroid6010 substrate

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