A NOVEL MDAC SUITABLE FOR A 14B, 120MS/s ADC, USING A NEW FOLDED CASCODE OP-AMP

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ABSTRACT

In this article, a 14bit MDAC, with 120Ms/s conversion rate that is simulated in 0.18 μ m CMOS technology is presented. The MDAC utilizes a new high speed, high gain op amp based on the well-known folded cascode structure. In this op amp, a new positive feedback structure is used to achieve a very high DC gain, while its unity gain bandwidth remains unchanged. In contrast with the conventional positive feedback schemes, the gain of the proposed op amp has a very low sensitivity to output swing. Its common mode rejection ratio is also improved by using the proposed structure.

KEYWORDS

ADC, MDAC, high speed, high gain, Op Amp.

1.INTRODUCTION

Data Converters are one of the most important parts in mixed mode systems and are considered as a bottleneck from the speed and resolution point of view. Pipelined analog to digital converters are now the best choice to provide high sampling rate with high resolution.

The performance of these systems is mainly limited by the settling behavior of a CMOS amplifier, due to the difficulty of designing a fast op amp with a very high dc gain. In some op amps such as telescopic and folded cascode op amps [1] [2], transistor cascoding is used to increase the output resistance and therefore to increase the dc gain of the Op Amp. However, telescopic structure suffers from a large voltage headroom drawback, making it not applicable to low voltage circuits. Moreover, in deep sub-micron processes, the intrinsic transistor resistance becomes smaller, thus the advantage of cascoding becomes more limited. Structures such as folded cascode op amps have medium dc gain. In two stages op amp high dc gain is produced by transistor cascading. However the second stage adds a pole, which causes a decrease in bandwidth. So these types of op amps can not settle fast enough. Enhancing the amplifier gain, through the use of the gain boosting technique is the other way of boosting the amplifier gain, without limiting the high frequency performance [3]. However boosting amplifiers add their own poles and zeros to the final amplifier which causes zero – pole doublets that affect amplifier settling and decreases its speed. Bulk driven cascode and folded cascode op amps are typically designed to overcome the signal swing problem [4]. Recent works utilize bulk driven transistors operating in weak inversion to obtain low voltage and low power amplifiers [5]. However the bulk driven topologies still suffer from the reduction in g_{mb}/g_m problem especially in the nanometer CMOS technologies. The final method used to increase the gain is the positive

feedback technique [6][7][8]. However, the gains of the most positive feedback circuits are strongly depend on transistor matching, which causes nonlinearity in the circuit.

Typical pipelined ADCs are classified into single bit-per-stage and multi bit-per-stage architectures. For more than 12b resolution, the multi bit-per-stage architecture is more suitable than the single-bit-per-stage architecture, which requires many stages, high power consumption, and a large chip area.

Figure 1. Architecture of the proposed 14bit ADC.

In 1996 Gil-Cho Ahn et. all described a 12-b, 10-MHz ADC [9], which consisted of four stages based on a multiplying digital-to-analog converter (MDAC). In 2004 Sang-Min Yoo et. all described a 10-b 120-MSample/s pipelined ADC [10] which used the merged-capacitor switching (MCS) technique to improve the sampling rate and the resolution of an ADC.

This paper describes a new MDAC [11] which can be used in a 14b, 120-MSample/s ADC, consisting of three stages based on a MDAC (Figure 1). Digital correction logic is inserted for correcting noncritical errors [12]. The MDAC utilizes a new fully differential folded cascode op amp, with a high differential gain and a high bandwidth. A brief explanation about the MDAC architecture is described in section 2. In section 3, the proposed folded cascode op amp with positive feedback is explained. The simulation results are shown in section 4. Conclusions are discussed in section 5.

2. MDAC ARCHITECTURE

The MDAC in each-stage is implemented by using a unit capacitor (UC) array [10] [11]. This unit capacitor based MDAC is directly driven by output from the flash ADC and not from the decoder, enabling it to switch more quickly.

Merged capacitor array is used [10], which merges two unit capacitors into one without affecting the performance of the remaining circuits of the ADC [11].

3. GAIN STAGE

In pipelined converters the high linear processing of the analog input relies heavily on operational amplifiers. The maximum allowable gain error and nonlinearity of the residue amplifier in each stage is proportional to the number of bits resolved afterward. Thus the worst case is in the first stage and maximum gain accuracy is required for the first stage. In our design consideration, after the first stage, the residue is equal to $2^{-4}V_{ref}$, which is entered into the gain stage and causes an error according to the gain stage error. This error must be smaller than the value of $1/2LSB$, relaxed by 3bit. So the maximum gain error which the system can tolerate, without a bit error occurring, α , must be smaller than 2^{-11} .

$$\alpha = \frac{1}{\beta} - \frac{A}{1 + A\beta} \quad (1)$$

Where $1/\beta$ is the inter-stage gain factor and equals to 2^3 and A is the op amp gain. In order to obtain this accuracy, the op amp gain must be greater than 84.3dB. In the differential case, the gain must be greater than half of the above value. Some margin larger than the above value is considered to tack care of process variation and mismatch errors. Some of the gain and offset errors of the op amp is corrected employing digital correction logic.

The MDAC must also operate in a time constraint, which is smaller than 9ns for operating in a 120Msample/s ADC. It is evident from the consideration above that a two stage Op Amp can not settle fast enough. Because the second stage adds a pole which causes a decrease in bandwidth, so a one stage Op Amp with 2 dominant poles must be considered.

To achieve high accuracy requirements for 14-bit pipeline ADC, unity frequency should be much larger than sampling frequency. The error which is produced by low bandwidth of the op amp should be less than 1/2 LSB of an ADC with the same reference voltage and resolution of remaining bits.

$$\left[\frac{1}{\beta} - \frac{1}{\beta} \times \left(1 - e^{-\frac{t}{\tau}} \right) \right] \frac{V_{ref}}{2^M} \leq \frac{V_{ref}}{2^{N-M+1}} \quad (2)$$

Figure 2. Initial idea of folded cascade op amp with positive feedback.

In the above equation, $1/\beta$ is inter stage gain, V_{ref} indicates the reference voltage of ADC and $1 - e^{\frac{-t}{\tau}}$ is the step response of feedback system with $\tau = \frac{1}{2\pi\beta f_u}$. The sampling frequency is 120MHz ($T_{\text{sampling}} = 8.3\text{ns}$). Therefore the time available for settling can be approximated as,

$$T_{\text{settling}} = \frac{3}{4} T_{\text{sampling}} \approx 6 \text{ ns} \quad (3)$$

For $N=14$, $M=4$ and $\beta=1/8$, the minimum gain-bandwidth required is 1.6 GHz.

3.1. Initial Idea

Figure 2 shows the initial idea of the proposed op amp. It is a folded cascode op amp with extra transistors, MFs, which are added at the output nodes to increase the op amp gain. Differential gain of the amplifier can be written as,

$$\frac{V_o}{V_i} = \frac{-gm_I R_O}{K} \times \frac{1}{1 + \frac{(R_{out} C_{load})}{k} s}, \quad k = 1 - gm_F R_O \quad (4)$$

Where gm_I is the input transistor transconductance, gm_F is the feedback transistor transconductance, and R_O is the output resistance.

As can be seen in (4), the differential dc gain is divided by the K factor, and the output dominant pole is multiplied by K. If $gm_F R_O = 1$ or if $K=0$, then the amplifier will exhibit an infinite dc gain. Note that no additional nodes or poles are added. However, this amplifier suffers from two drawbacks.

Figure 3. (a) Proposed Operational Amplifier (b) Half circuit of proposed Op Amp

Figure 4. Half circuit of proposed Op Amp in common mode state

(a) The gate of feedback transistors (MFs) are directly connected to the output node. In wide swing operation, gm_F will be a strong function of output signal. Therefore, the dc gain of the amplifier will change widely, as the output node swings up or down. This phenomenon causes nonlinearity in the circuit.

(b) As can be seen in (4), if $K < 0$, then the dominant pole will be in the right half plane and the op amp becomes unstable. The value of $gm_F R_O$ can easily be greater than one. Therefore, it is very probable that the circuit of Fig. 1 will become unstable.

To alleviate these two problems, a modified version of the above op amp is proposed in the next section.

3.2. Proposed Op Amp

Figure 3(a) shows the modified version of Figure 2, with two transistors ML_1 and ML_2 , are added to the circuit. These transistors, which are operated in the triode region, act as degenerative resistors at the source of MF transistors. Therefore, the feedback loop gain can be adjusted to a desirable value by selecting suitable size of these transistors. Furthermore, the linearity of the circuit will be improved by adding these two transistors.

A common mode feedback circuit, is inserted to the proposed differential op amp to adjust the common mode voltage, around the desired value [6].

3.3. Differential Mode Gain

A half circuit of the op amp is shown in Figure 3(b). The output resistance (R_O) in Figure 3(b) is equal to $R_{up} \parallel R_{down}$. By considering $r_{eq} = r_{ds1} \parallel r_{df} \parallel r_{ds10}$, where $r_{df} = r_{dsf} + R$, and considering

$$Gm_f = \frac{gm_f}{(1 + gm_f R)} \text{ in Figure 4(b), and writing KCL on node } V_c, R_{down} \text{ are given by,}$$

$$R_{down} = \frac{r_{ds8} + r_{eq} + gm_8 r_{eq} r_{ds8}}{1 - Gm_f r_{eq} - Gm_f gm_8 r_{eq} r_{ds8}} \quad (5)$$

By

ignoring r_{ds8} and r_{eq} in comparison with $gm_8 r_{eq} r_{ds8}$ and $Gm_f r_{eq}$ in comparison with $Gm_f gm_8 r_{eq} r_{ds8}$ and considering $gm_8 r_{eq} r_{ds8} = A$, and simplifying the value of Gm_f , to the value of $1/R$, (5) is simplified to (6).

$$R_{down} = \frac{A}{1 - A/R} = \frac{AR}{R - A} \quad (6)$$

The value of R_{up} , which is equal to $gm_6 r_{ds6} r_{ds4}$ is considered as B , so the value of R_O , can be calculated as,

$$R_O = R_{up} \parallel R_{down} = \frac{ARB}{AR + BR - AB} = \frac{A \parallel B}{1 - (A \parallel B)/R} = \frac{A \parallel B}{K_d} \quad (7)$$

The total transconductance of the circuit is equal to gm_1 . Therefore the differential gain of the proposed op amp is,

$$\frac{V_O}{V_I} = \frac{-gm_1 (A \parallel B)}{K_d} \quad (8)$$

Where $A \parallel B$ is the output resistance of a conventional folded cascode op amp, and K_d is a factor, that is proportional to the value of R , which is the output resistance of triode region transistors ML_1 and ML_2 , and also is proportional to the value of $A \parallel B$. The gates of two triode region transistors, ML_1 and ML_2 , are connected to the output signal (Figure 3(a)). Therefore the value of R is equal to,

$$R = \frac{1}{2 \left(\mu C_{ox} \frac{W}{L} ((V_{b1} + V_{b2}) - (V_{out+} + V_{out-}) - 2V_{TH}) \right)} \quad (9)$$

In (9), $(V_{b1}+V_{b2})$ and $(V_{out+} + V_{out-})$ are constant values, so the value of R is constant and can be adjusted by adjusting the size of W/L . By selecting appropriate ML_1 and ML_2 sizes, parameter K_d can be controlled so that it obtains a value between zero and one.

As can be seen in (8), the gain of the proposed op amp is equal to the gain of a conventional folded cascode op amp divided by the value of K_d . With considering the value of K_d , sufficiently small, the gain of op amp will increase considerably.

So in spite of the conventional Op Amps, we don't have to increase the output resistance to increase the gain. In this structure, if the output resistance be a little smaller than R , gain will increase considerably. A large value of R , also improves the linearity of the circuit. Another advantage of this architecture is that the differential gain of the op amp does not depend on gm_f , so it does not depend on the output node variation.

3.4. Common Mode Gain

In the common mode state, the positive feedback is converted to a negative feedback. Therefore, the common mode gain of the proposed amplifier is less than the common mode gain of a conventional folded cascode amplifier.

The half circuit of proposed op amp in common mode state is shown in Figure 4. The value of R_O , which is the output resistance of the op amp in common mode state, is obtained in a similar manner, as bellow.

$$R_{down} = \frac{r_{ds8} + r_{eq} + gm_8 r_{eq} r_{ds8}}{1 + Gm_f r_{eq} + Gm_f gm_8 r_{eq} r_{ds8}} \approx \frac{gm_8 r_{eq} r_{ds8}}{1 + Gm_f gm_8 r_{eq} r_{ds8}} \quad (10)$$

Where $r_{eq} = r_{ds10} || (2gm_1 r_{ds1} r_{ds1}) || (gm_F r_{dsF} r_{ds13}) \approx r_{ds10}$ and $Gm_f = gm_F / (1 + gm_F r_{ds13}) \approx 1/r_{ds13}$. By considering, $gm_8 r_{eq} r_{ds8} = A$, the value of R_{down} is obtained as below,

$$R_{down} = \frac{A}{1 + A/r_{ds13}} = \frac{A r_{ds13}}{A + r_{ds13}} \quad (11)$$

The value of R_{up} , which is equal to $gm_6 r_{ds6} r_{ds4}$ is considered as B , so the value of R_O , can be calculated as,

$$R_O = R_{up} || R_{down} = \frac{A || B}{1 + [A || B] / r_{ds13}} \quad (12)$$

Where $A || B$ is the output resistance of a conventional folded cascode op amp. The transconductance of the circuit in the common mode state, is equal with,

$$Gm_I = \frac{gm_1}{(1 + 2gm_1 r_{ds1})} \quad (13)$$

And the common mode gain of the proposed op amp is,

$$A_{vcm} = \frac{V_o}{V_{cm}} = \frac{-gm_I}{1 + 2gm_I r_{ds1}} \cdot \frac{A||B}{1 + [(A||B)/r_{ds13}]} \quad (14)$$

3.5. Common Mode Rejection Ratio

The CMRR of proposed op amp is obtained as in (15).

$$CMRR = \frac{(1 + 2gm_I r_{ds1}) [1 + ((A||B)/r_{ds13})]}{K_d} \quad (15)$$

Where,

$A||B$ is the output resistance of a conventional folded cascode op amp. As can be seen in (15), the rate of an increase in common mode rejection ratio, is the same as that of the differential gain. However this is not true about conventional folded cascode op amp.

3.6. Frequency Response

The proposed op amp has two major poles. The dominant pole occurs at the output node and the non dominant pole occurs at the cascode node.

Figure 5. (a) A comparison between the proposed and conventional folded cascode op amp (Gain and Phase). (b) Step response of amplifier to a 50mV step.

The dominant pole, p_1 is equal to,

$$P_1 = \frac{-1}{R_o C_{Load}} = \frac{-1}{\frac{A||B}{1 - [(A||B)/R]} C_{Load}} \quad (16)$$

If $R < A||B$, then the dominant pole, is in right half plain and op amp becomes unstable. To avoid this, the value of R must be a little bigger than the value of $A||B$. So the dominant pole decreases and the op amp becomes more stable.

The nondominant pole, is equal to,

$$P_2 = \frac{-1}{r_{eq} || 1/gm_8 C_{ncas}} \quad (17)$$

where n_{cas} is the cascode node (drain of M10 and M11).

P_2 is almost equal with the nondominant pole of a conventional folded cascode op amp.

As can be deduced from above discussion, the gain of the proposed op amp increases considerably compared with a conventional folded cascode op amp, while its unity gain frequency remains almost unchanged.

3.7. Simulation Results

The post layout SPICE simulation results related to the proposed circuit are shown in this section. Figure 5(a) shows the simulation results of the proposed op amp with the load capacitance of 0.15PF.

In Figure 5(a), the dc gain of the conventional folded cascode op amp is about 32dB. By adding the feedback loop as described in this paper, the dc gain of the proposed op amp increases to the value of approximately 92dB. Therefore, the dc gain increases while 3dB frequency bandwidth decreases. The phase margin of the proposed op amp is about 76° , which is a decrease about 6° , relative to the conventional folded cascode op amp. Unity gain frequency of the op amp is about 1.6GHz at 0.15PF load capacitance. Figure 5(b) shows the step response of the amplifier to a 50mv step, which is 5.6ns. THD of the Op Amp for different output swings in unity gain configuration is presented in Figure 6(a). The specification of proposed op amp is summarized in Table 1.

Figure 6 (a)THD of the Op Amp for different output p-p swings in unity gain configuration. (b) Simulation results of MDAC.

4. MDAC SIMULATION RESULTS

The designed MDAC is simulated to operate with a maximum 0.8V input signal swing with a 1.8V supply voltage. The maximum residue is $0.8 \times 2^{-4} = 50\text{mV}$. Figure 6(b) shows the simulation results of MDAC when bits are detected correctly with flash comparators. These results indicate that the gain error is less than 0.3mV. The MDAC settling time is 7ns. This time includes times for sampling, subtracting and amplifying. Table 2 shows the performance summary of the MDAC. The Layout pattern of the proposed MDAC is illustrated in Figure 8.

Table 1. Summarizes the Specifications of the Proposed Op Amp.

Process	0.18 μ m
Supply Voltage	1.8V
Open Loop Gain	92dB
DC Gain Enhancement	60dB
Unity Gain Frequency	1.6GHz
Phase Margin @ 0.15PF	76°

Table 2. Performance Summary of the MDAC.

Process	0.18 μ m
Supply Voltage	1.8V
Resolution	14B
Conversion rate	120MS/s
Input Range	.8V
settling time @ 0.15PF	7ns
Power Dissipation	7. 8mW

Figure 8. Layout of the proposed MDAC

5. CONCLUSIONS

This paper has presented a MDAC which is suitable for a pipelined ADC, with a 14bit of resolution and a 120Msample/s conversion rate in 0.18 μ m CMOS technology. The power consumption of this MDAC is 7.8mw and its settling time is 7ns. The MDAC utilizes a new structure for the folded cascode op amp, which uses the positive feedback scheme. The dc gain of the op amp and also the common mode rejection ratio is increased by about 60dB, with this proposed method. Two regenerative resistors are added to the op amp circuit to improve the linearity of the circuit. The proposed feedback scheme is only positive in the differential mode and in the common mode state reverts back to a negative feedback. Unity gain frequency of the op amp is about 1.6GHz and the phase margin of the proposed op amp is about 76° at 0.15PF.

Through the use of a one stage op amp the power consumption is reduced and its speed is increased. Furthermore by using a new topology, a high gain is obtained, which is necessary for a 14bit resolution in an ADC.

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