Barriers in Miniaturization of Electronic Devices and the Ways to Overcome Them — from a Planar to 3D Device Architecture

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We witness a new revolution in electronic industry — a new generation of integrated circuits uses as a gate isolator HfO_2 . This high- k oxide was deposited by the atomic layer deposition technique. The atomic layer deposition, due to a high conformality of deposited films and low growth temperature, has a large potential to be widely used not only for the deposition of high- k oxides, but also of materials used in solar cells and semiconductor/organic material hybrid structures. This opens possibilities of construction of novel memory devices with 3D architecture, photovoltaic panels of the third generation and stable in time organic light emitting diodes as discussed in this work.

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1. Introduction

According to Gordon Moore, cofounder of the Intel company, we witnessed in 2007 a new revolution in the electronic industry, comparable to the one related to the introduction of integrated circuits (ICs). In ICs introduced by the Intel company in the Autumn 2007 SiO_2 was replaced by HfO_2 as a gate isolator. This enabled introduction of the ICs with 45 nm node and further scaling of dimensions of CMOS transistors to the 32 nm node (expected at the end of 2009) and then to the 22 nm node.

Further scaling down likely requires change of the IC device architecture. In this paper we discuss perspectives of further increase of capacity of electronic devices by an introduction of devices with a 3D architecture. We analyze expected consequences of the introduction of this new architecture in electronic devices.

2. Miniaturization of electronic devices

According to the law formulated by Moore [1] number of transistors in ICs doubles approximately every two years, resulting in 10^9 transistors in the ICs prepared with the 45 nm node technology. Scaling down of CMOS transistors in ICs resulted however in serious problems. Reduction of the gate length from 1 μm in the 1974 transistor to about 35 nm in the 2005 Intel transistor enabled a reduction of the operating voltage from 4 V to 1.2 V, but led to a reduction of thickness of gate dielectric (SiO_2

based) from 35 nm to 1.2 nm. The latter resulted in a rapid increase of a tunneling current by 4 orders in the magnitude, questioning the possibility of a further miniaturization of CMOS transistors in ICs.

This problem was solved by the Intel company by introduction a high- k oxide (HfO_2) as a gate dielectric [2]. Use of the HfO_2 enabled, while keeping the same operating voltage, an increase of isolator thickness from 1.2 nm to 3 nm. The leakage current was reduced on this way by the two orders in magnitude, opening chances for further miniaturization of ICs. Gate dielectric was deposited by the atomic layer deposition (ALD), due to unique properties of this growth method, described shortly below.

3. Technique of the atomic layer deposition

The ALD is a self-limiting growth process, introduced in 70-ties by Suntola from Finland [3]. The key property of the ALD is sequential introduction of reaction precursors (usually organic ones). A pulse of the first one saturates a surface of the growing film. Then gases of an unused precursor are purged away from a reactor, with a pulse of a neutral gas. Only then the second precursor is introduced to a growth chamber, reacting with the first precursor adsorbed at the surface of the growing film. In the consequence, the precursors never meet in a gas phase and thus their pre-growth reactions are avoided. This means that in the ALD very reactive precursors can be used, which are not suitable for the use in CVD (metal-organic chemical vapor de-

position (MOCVD), metal-organic vapor phase epitaxy (MOVPE)) processes.

Use of very reactive precursors means that the ALD enables growth at low temperatures. Moreover, due to the growth mode with a surface saturation, the ALD enables very uniform covering of 3D structured surfaces. For the application in ICs two other advantageous properties of the ALD turned out to be the most important. First, high conformality of the films deposited with the ALD, meaning that structured surfaces can be uniformly covered. Second, high density of thin films deposited with the ALD. The latter means that fairly thin HfO_2 films show a dielectric constant similar to the one expected for thick (bulk) layers of HfO_2 , which was not the case when other growth/deposition techniques were used.

Such property of HfO_2 films was confirmed by our study, in which we used tetrakis(dimethylamido) hafnium(IV) and deionized water as hafnium and oxygen precursors

Temperature window of growth of HfO_2 , as determined by us, was in the range of 130–140°C. The so-obtained films of HfO_2 were very flat and polycrystalline, despite a fairly low growth temperature.

4. New trends, new architecture

The replacement of SiO_2 by high- k oxides means that the important advantage of Si (SiO_2 as a gate dielectric) for use in electronics is gone. Especially since, in the accordance with our experience, HfO_2 layers can be easily deposited by the ALD on different substrates, including GaAs. Thus, a new generation of electronic devices may use other than Si materials, especially these with higher electron and hole mobilities. Higher mobilities mean higher operation speeds of ICs, which are expected for III–V-based structures (for electrons) and Ge (for holes).

As already mentioned, introduction of high- k oxides enabled reduction of a leakage current by two orders in the magnitude, opening chances for further miniaturization of CMOS transitions to 32 nm and then 22 nm node. For further increase in ICs capacity we need another approach.

In fact, recent improvements in ICs performance were related to miniaturization of sizes of CMOS transistors. This soon will not be possible due to technological reasons and also will be too expensive. Further increase in ICs capacity/performance requires thus another approach. A 3D architecture of electronic devices is now tested, as described below on the example of so-called cross-bar memories, which, if mastered, will enable further increase in a storage density of memory devices.

4.1. Concept of cross-bar memories

Non volatile semiconductor-based RAM memories use concept of a floating gate, introduced by Masuoka

in 1984. Their structure is nearly identical with the one used in field effect transistors in ICs. One extra gate is added (floating gate) embedded in a gate isolator. This similarity to CMOS transistors means that they closely follow development of these transistors in ICs and that floating gate memories can further be scaled down following the trend in ICs.

A new concept (a new architecture) is now tested in order to increase further a storage density, above the one achieved by miniaturization to 45 nm, and then 32 nm and finally 22 nm node. One of the tested post-floating gate architectures is a cross-bar memory one. This is a 3D structure, with vertically stacked memory cells (see e.g [4, 5]). The storage density of such memory devices increases with the decrease of the value given by the $4F^2/n$ equation. In this equation F is a node standard (e.g. 65 nm) and n is number of stacks. To compete with the present storage capacity of floating gate memories we need at least three stacks of memory cells, meaning that a fully 3D structure is required.

4.2. Why not silicon?

Importantly, construction of 3D electronic devices means a revolutionary change in device processing and imposes serious material and processing restrictions. Till now the front of line approach was used to construct ICs and memory cells, with a planar construction of ICs and metallization on top of these devices. This must be changed if 3D stacks will be introduced to electronic devices. Metal paths will be both beneath and above transistors/memory cells, which drastically restricts growth temperature to below 350–400°C [4, 5]. This restriction is difficult to be realized in a “classical” silicon technology. Thus, it is now seriously considered that new 3D devices may not be based on silicon.

In the frame of the VERSATILE European project we demonstrated that ZnO can be material of choice for the cross-bar memories applications [4, 5]. In the approach tested by us we used ZnO as material for a so-called selector in a memory cell. Each memory cell consisted of a selector (junction enabling writing and reading of individual cells) and memory storage element — so-called anti-fuse. As the latter we tested several possibilities — organic material, NiO or phase change memory element [4, 5].

By using the ALD we achieved a low temperature of ZnO deposition, which was required in the back-end of the line (BEOL) architecture of the cross-bar memories. As zinc precursor we used diethylzinc (DEZn) with deionized water used as an oxygen precursor [5–9]:

Growth temperature was reduced to about 100°C, enabling not only construction of selectors (Schottky or p – n diodes), but also of hybrid structures of the type ZnO/organic material [10], as described further on.

Important advantage of the ALD growth was high quality of the deposited ZnO films. Even though polycrystalline ZnO films were obtained, when grown at a

low temperature, these films show relatively high electron mobility (typically of $10\text{--}50\text{ cm}^2/(\text{Vs})$), better than these reported for polycrystalline Si films (commonly below $10\text{ cm}^2/(\text{Vs})$). Moreover, a high forward current density, which enabled to read and write information using various tested storage elements, and a high rectifying ratio (i.e. a low leakage current) were achieved. The latter was essential for addressing of selected memory cells, without current passing through the other non-selected cells [4].

5. Hybrid ZnO/organic material structures

For organic materials one must solve problem of their time stability. Otherwise, they will never be serious competitors of semiconductors in electronics, optoelectronics and solar cells. Time stability of organic-based devices can be improved by their coating with transparent wide band gap materials. This was recently demonstrated for organic solar cells [10, 11]. Such coating, performed on top of organic material, requires a low thermal budget of a growth and of a post-growth treatment, making the ALD an attractive growth method.

Low growth temperature (well below 200°C) and high conformality of ZnO grown by the ALD enabled us testing of several ZnO/organic material structures for electronic, optoelectronic and photovoltaic (PV) applications [6, 10]. The latter application is very promising and as such will be shortly described below.

5.1. ZnO by the ALD for solar cells applications

In 1954 Bell Laboratories developed the first PV cell based on a monocrystalline silicon. This was the prototype of the first generation of PV cells — $p\text{--}n$ junction of a monocrystalline Si. Unfortunately, a payback time for this generation of solar cells is very long — 25–30 years, which is comparable with their lifetime. This is why other materials and structures are extensively studied in order to either increase PV cells efficiency, or to reduce their costs [6, 12, 13].

Selection of growth conditions allowed us to obtain ZnO films by the ALD with n -type doping of 10^{20} cm^{-3} and with a relatively high electron mobility of about $30\text{--}40\text{ cm}^2/(\text{Vs})$ [6, 9, 13], making them suitable for applications as transparent electrodes in PV devices and in organic light emitting diodes (OLEDs).

In particular, application in the so-called third generation of solar cells is aimed by us. Third-generation of solar cells uses organic/polymer materials, with their costs reduced to a few \$ per m^2 . Such PV cells stable in time were constructed by us by coating of organic material [6, 10]. In such application ZnO acts not only as a transparent electrode, but also helps to reduce environment effects, stabilizing an organic material. Importantly, as demonstrated by us [10], coating with ZnO results in a junction with a high rectification ratio. This was recently demonstrated by us for P3HT/ZnO system [10]. Good

electrical parameters of the junction ensure effective separation of photoexcited carriers in PV cells.

6. Conclusions

In the present study we discuss ways of further miniaturization of electronic devices by either introduction of high- k oxides as gate isolators or by development of structures with a 3D architecture. The latter was described on example of developed by us cross-bar memories. We discuss also advantageous properties of ZnO films grown by the ALD using organic zinc precursors. Such films are suitable for applications in hybrid structures of the type semiconductor/organic material, which may be used in novel optoelectronic and photovoltaic devices.

Acknowledgments

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