DLC Coatings by PI³D: Low-Voltage versus High-Voltage Biasing

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Diamond-like carbon (DLC), in particular hydrogenated amorphous carbon (a-C:H) films have been formed on various conductive and dielectric materials by plasma immersion ion implantation and deposition (PI³D) processing. Effect of pulse voltage and other process parameters on the film properties was investigated. It was found that for conductive substrates, a low-voltage (≈ 1 kV), high repetition rate pulsing provides better overall film performance comparing to that obtained by applying higher voltages, which is also favourable for conformal treatment of 3D workpieces. However, short 1–2 μ s, high-voltage 5–20 kV pulses are required for dielectric workpieces several millimeter thick. Good film adhesion was achieved by forming a Si-containing buffer layer using hexamethyldisiloxane (HMDSO) as a precursor and a low-voltage pulsing. Roughness and wettability of DLC coatings was found to be controlled by varying the bias specs and sample temperature. Very smooth films with average roughness less than 1 Å were prepared at optimised process parameters.

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1. Introduction

Formation of diamond-like carbon (DLC) film, in particular hydrogenated amorphous carbon (a-C:H), requires energy delivery about 100 eV per deposited carbon atom during plasma processing [1]. The condition generally can be fulfilled using either DC or pulse mode providing the ion energy during pulse $E_{ip} = E_{iDC}/(\tau_p \cdot f)$, where τ_p is the pulse width, and f is the pulse repetition rate (PRR). It implies that even high energy pulsed ion bombardment can be used for DLC formation. Plasma immersion ion implantation and deposition (PI³D) is a pulsed bias technique well suited for preparation of DLC coatings [2–5]. Pulsed biasing, comparing with RF self bias, commonly used in DLC processing by plasma-enhanced chemical vapor deposition (PECVD), allow treatment of thick (up to ≈ 10 mm), large-area dielectric materials using short, high-voltage pulses as well as formation of low-stress coatings at certain operational conditions [6]; preparation of DLC coating with higher annealing temperature.

In this paper, DLC coatings were formed on various conductive and dielectric substrates using a 100 l, 60 kV PI³D system MM-100/60 (KERI), equipped with an interior-antenna inductively coupled plasma (ICP) source [7, 8]. Dependence of the film properties on pulse voltage and other process parameters is discussed.

2. Experiment

The layout view of the PI³D system is shown in Fig. 1a. A 2 kW, one-turn interior RF antenna ICP source pro-

vides uniform plasma in a 100 l cylindrical chamber with density up to 10^{11} cm⁻³. Acetylene (C₂H₂) and toluene (C₆H₅CH₃) alone or with argon were used as precursors for DLC formation, hexamethyldisilazane (HMDSA) and hexamethyldisiloxane (HMDSO) were applied to prepare Si-containing buffer layer, while the same precursors in certain proportion with toluene were used to deposit Si-DLC films. Operational pressure was 0.5–2 mTorr. Choice of both ICP power (i.e. plasma density) and pulse biasing was based on the measured plasma parameters and predictions of the plasma immersion ion implantation (PI³) model [7, 9]. To provide conformal treatment of 3D conductive workpieces, higher plasma density $(5\text{--}10) \times 10^{10}$ cm⁻³ and low voltage 0.5–1 kV at high PRR 10–70 kHz were used. In a case of such small pulse amplitude, the pulse width, τ_p , has a minor effect on the coating conformity because the sheath almost reaches a steady-state Child extent within just $(10\text{--}20)\omega_{pi}^{-1}$, where ω_{pi} is the ion plasma frequency [9]. Therefore τ_p was 3–10 μ s in this case. Typical oscillogram of pulsed bias and load current is shown in Fig. 1b. However, for dielectric substrates short pulses of 1–1.5 μ s were used to minimize surface charging during the pulse and hence, substrate damage and decreasing of the ion impinging energy [10]. The latter implies using higher pulse voltage and smaller plasma density. For thick dielectric (of 5–10 mm thickness) reduction of dielectric-to-sheath capacitance ratio requires further increase of pulse voltage. Depending on the substrate, we applied 2–10 kV pulses at PRR of 2–50 kHz. The pulses featured short rise time, 0.1–0.3 μ s, and fall time, 0.3–1.2 μ s, to min-

Fig. 1. (a) Layout view of a 100 l, 60 kV PI^3D system MM-100/60. (b) Typical oscillogram of pulsed voltage (upper trace, 500V/div) and load current (lower trace, 5 A/div) during DLC processing.

imize ion bombardment of a substrate with undesired energies, to weaken surface etching and heating, and to reduce plasma restoration time [8].

The workpiece temperature was monitored by a thermocouple. Although the workpiece stage was water cooled, in some experiments the cooling was turned off to extend temperature range although temperature did not exceed 200°C in all cases.

To analyze the coating properties, the films were grown on planar polished substrates of Si (100) $p(B)$ -type; glass (bare and Cr-coated); Al6061 (bare and Cr coated); WC-Co (P30) alloy. The DLC structure was evaluated from the Raman spectra (Renishaw, Invia Reflex, 514 nm). Field emission scanning electron microscope (FE SEM) (FEI, Siron) was used to analyze surface morphology, interface, and growth mode. The film surface roughness was measured with atomic force microscope (AFM) (PSIA, XE-100). The hardness (H) and Young's modulus (E) of the films on silicon samples were characterized by nanoindentation (MTS, Nano Indenter XP) with Berkovich diamond tip using both, conventional and continuous stiffness mode. Wettability of the coatings was characterized by the surface energy evaluated from the contact angle measurements (Kruss, DSA10). Thickness of DLC and Si-DLC coatings was 1–2 μm in all cases.

3. Results and discussion

Subplantation mechanism of DLC formation is responsible for increase fraction of C–C sp^3 bonds and, consequently, hardness [1]. Insufficient ion bombardment leads

to the film polymerization, while excess irradiation causes graphitization. If high energy, pulsed ion flux is used for DLC formation, thermal spikes and extended range of ion energy loss in the matter may decrease maximum film hardness and shift the value of E_0 . Figure 2 reflects these previous observations. It shows dependence of nanohardness of a-C:H films prepared on Si at different values of $V_p \tau_p f$. Pulse voltage was in the range of 0.2–1.0 kV for all points but that marked as the filled circle, for which $V_p = 5.0$ kV. Other conditions are displayed in the figure. It is seen that the film hardness has well pronounced maximum of 18 GPa at around 100 V. However, hardness of the film deposited at 5 kV is twice less, which is attributed to the upper mentioned factors. The 5 kV point belongs to the right shoulder of the corresponding curve. This is also confirmed by the value of $E_i j_i / j_0$ estimated using the film density derived from the corresponding Raman spectrum. Here j_i and j_0 are ion and neutral flux densities, respectively. Deposition rate of 4 $\mu\text{m}/\text{h}$ was obtained for DLC films with hardness of 5 GPa, while only the value of 0.5 $\mu\text{m}/\text{h}$ for 20 GPa coatings prepared using toluene as a precursor, which is attributed to higher film density in the latter case. Comparing with DLC, higher deposition rate was reported for Si-DLC [11]. However, our results did not reveal marked difference at least within the parameters range used.

Fig. 2. Hardness of DLC coatings as a function of product of pulse voltage, V_p , pulse width, τ_p , and pulse repetition rate, f . Filled squares correspond to $V_p = 0.2$ –1.0 kV; filled circle — to $V_p = 5.0$ kV. Dashed line is a guide for the eye.

DLC films deposited at different process parameters demonstrate different wettability. Water contact angle was between 70°–110°. Generally, the higher angle corresponds to higher pulse voltage. One of the factors affecting hydrophobicity of the prepared DLC films is the surface roughness. Typically it was $R_a \approx 0.1$ –0.8 nm, which is comparable with similar film prepared by other techniques [12]. However, at certain process parameters it was much higher, up to 40–60 nm. Figure 3 shows cross-section FE SEM images of two DLC films deposited on Si substrate under the same conditions but temperature. While sample (b) was water cooled and thus had

lower temperature, the sample (a) was not cooled. As seen from the figure, the sample (a) has dense structure; the film hardness is 16 GPa. However, sample (b) is porous and soft ($H = 8$ GPa). Films like that in Fig. 3b could be formed at lower process temperature using mixture of toluene and argon, and bias voltage of ≈ 1 kV.

Fig. 3. Cross-section FE SEM image of DLC film on Si. Samples (a) and (b) were prepared at the same process parameters but temperature: $\approx 180^\circ\text{C}$ and $\approx 80^\circ\text{C}$, respectively. Si-containing buffer layer is clearly seen.

Fig. 4. AFM image of very smooth DLC film on Si with $R_a = 0.72$ Å.

Figure 4 shows an AFM image of very smooth DLC film on Si substrate, prepared at optimum process parameters. The film hardness is 17 GPa. Such coatings are prospective for application in nanopattern transfer technology.

4. Conclusion

PI³D processing was performed to prepare adhesive DLC coatings having Si-containing buffer layer, and Si-DLC films with tailored properties on a number of conductive and dielectric materials. Effect of pulse voltage on the coating properties was investigated. It was found that use of high voltage (≈ 10 – 20 kV) is required for coating of thick dielectric materials, however for conductive materials using much lower, ≈ 1 kV, voltage at high repetition rate provides better overall coating performance. The film roughness and wettability can be controlled by variation of pulsed bias amplitude and sample temperature. Very smooth DLC films with average roughness of less than 1 Å were deposited at optimum process parameters which makes the processing attractive for large-size nanopattern transfer technology [13, 14].

References

- [1] J. Robertson, *Mater. Sci. Eng. R* **37**, 129 (2002).
- [2] K.C. Walter, M. Nastasi, C. Munson, *Surf. Coat. Technol.* **93**, 287 (1997).
- [3] D.H. Lee, X.M. He, K.C. Walter, M. Nastasi, J.R. Tesmer, M. Tuszewski, *Appl. Phys. Lett.* **73**, 2423 (1998).
- [4] K. Voltz, K. Baba, R. Hatada, W. Ensinger, *Surf. Coat. Technol.* **136**, 197 (2001).
- [5] G. Thorwarth, C. Hammerl, M. Kuhn, W. Assmann, B. Schey, B. Stritzker, *Surf. Coat. Technol.* **193**, 206 (2005).
- [6] K. Wazumi, Y. Koga, A. Tanaka, *Diamond Relat. Mater.* **12**, 1018 (2003).
- [7] S.A. Nikiforov, J.H. Kim, G.H. Rim, in: *Proc. 3rd Asian Particle Accelerator Conference (APAC'04), Gyeongju (Korea) 2004*, Pohang Accelerator Laboratory, Pohang 2005, p. 693.
- [8] G.H. Rim, *Surf. Coat. Technol.* **201**, 6495 (2007).
- [9] S.A. Nikiforov, G.H. Kim, G.H. Rim, *IEEE Trans. Plasma Sci.* **31**, 94 (2003).
- [10] T.W.H. Oates, M.M.M. Bilek, *J. Appl. Phys.* **92**, 2980 (2002).
- [11] L. Zajickova, V. Bursikova, V. Perina, A. Mackova, J. Janca, *Surf. Coat. Technol.* **174**–**175**, 281 (2003).
- [12] X.L. Peng, Z.H. Barber, T.W. Clyne, *Surf. Coat. Technol.* **138**, 23 (2001).
- [13] M. Maharizi, D. Peleg, A. Seidman, N. Croitoru, *J. Optoelectronics Adv. Mater.* **1**, 65 (1999).
- [14] S. Ramachandran, L. Tao, T.H. Lee, S. Sant, L.J. Overzet, M.J. Goeckner, M.J. Kim, G.S. Lee, W. Hu, *J. Vac. Sci. Technol. B* **24**, 2993 (2006).