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A 75 μW Two-Stage Op-Amp using 0.18 μW CMOS Technology for High-Speed Operations

K. Shashidhar[a,*], Sreenivasa Rao Ijjada[b] and B. Naresh[b]

[a]Guru Nanak Institutions Technical Campus, Department of Electronics and communication Engineering, Ibrahimpatnam, Telangana, India

[b]GITAM University, Department of Electronics and communication Engineering, Visakhapatnam, India

Low voltage operated Analog and digital circuits have big demand due to its better performance. But, it leads to number of challenges. Operational amplifier is the basic element in most of the circuits, because of its wide advantages. Gain, bandwidth, linearity, noise and output swings are the design parameters. Operational amplifier design is unique for different applications. This paper presents the design of a 1.8V two-stage Operational amplifier using 0.18 μm CMOS technology for low power and high-speed operations. This design draws 5 μA current with 1.8 V and produced the gain of 87 dB, phase margin (PM) of 67° and the unity gain bandwidth (GBW) of 4.87 MHz through AC analysis. The proposed design has a Slew rate of 4.126 V/μs, which determines the speed of the Operational amplifier. The input common mode range (ICMR) is improved to 0.07–1.65 V and the power dissipation is 75 μW.

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PACS/topics: operational amplifier, low power, gain, phase margin, unity gain bandwidth

1. Introduction

Operational amplifier (op-amp) gain decides the accuracy of analog to digital convertors (ADC) and switched capacitor circuits and settling behaviour and slew rate. CMOS technology advances give the scope of shrinking the transistor channel length such that it impacts in reducing the intrinsic gain and the DC gain also [1]. Conventional techniques such as cascoding and gain boosting will improve the gain. However, the design for low voltages these techniques are not fit because of limited voltage headroom. The gain can be improved by cascading of multiple gain stages [2]. The tradeoff between op-amp speed, gain, power and other such parameters presented in [3, 4]. All these are with the cost of stability in the closed loop due to the presence of high impedance nodes at each gain stages, hence producing the negative phase shift and consequently degrades the overall PM. In order to achieve stability in the closed loop, multi stages needs a compensation circuit to attain a minimum PM of 45°. Larger PM leads to produce less ringings at the output and smaller PM results more ringings at the output which affects the stability, hence the PM is preferred to be in range of 45° and 60°.

2. Design of op-amp circuit

The two two-stage op-amp circuits presented in [5, 6] have designed 1.8 V using 0.18μm technology suffering with low gain and PMs, hence in this paper proposed an op-amp circuit as in Fig. 1. In the design, initially

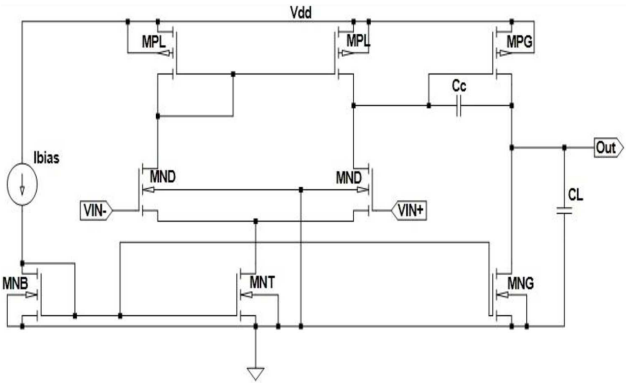

Fig. 1. Basic Two Stage Operational Amplifier.

select the compensating capacitor in such that with considerable amount of PM, i.e. for PM should be greater than 60°. With this a zero can be kept far away from the origin to maintain the system stability, hence assume $Z \geq 10$ (GBW) and use the condition $C_C \geq 0.22C_L$ [7]. For the desired value of compensation capacitance, find the current that is fed to a tail current using the formula $I_5 = SRC_C$. The tail current is used to split the current in the two sides of the op-amp. Then, calculate the gain using the formula $Av = g_m R_D$, where $R_D = 1/\lambda I_D$ manually by taking the transconductances either $gm1$ or $gm2$. Hence there is an insight that how much gain is coming close to the desired given design specifications. The value of transconductance gm1 is calculate with the formula, $gm1 = GBWCC2\pi$. Based on this value the aspect ratios of the NMOS transistors are selected. Then the PMOS transistors aspect ratios are calculated. Maximum ICMR voltage used in finding the aspect ratios. The main aim is to keep all transistors in saturation. The tail current also serves as a critical thing we should

*corresponding author; e-mail: shashignitc2015@gmail.com

design to keep in saturation we use input common mode voltage minimum and calculate the aspect ratio. Common source stage is the second stage for providing ample amount of gain. For this we design transconductance of transistor is very large than the transconductance of the input nmos transistors i.e. $gm6 = 10gm1$.

Finally, all these calculated values are used in the op-amp design and simulated for meeting the desired specifications.

3. Results and analysis

The circuit under goes for the AC testing after creating a symbol in Cadence Virtuoso editor as shown in Fig. 2.

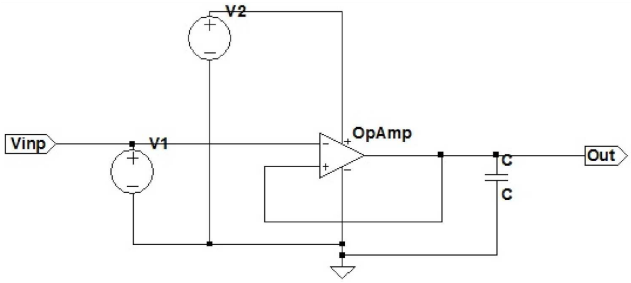

Fig. 2. Open Loop Gain Analysis of Op-Amp.

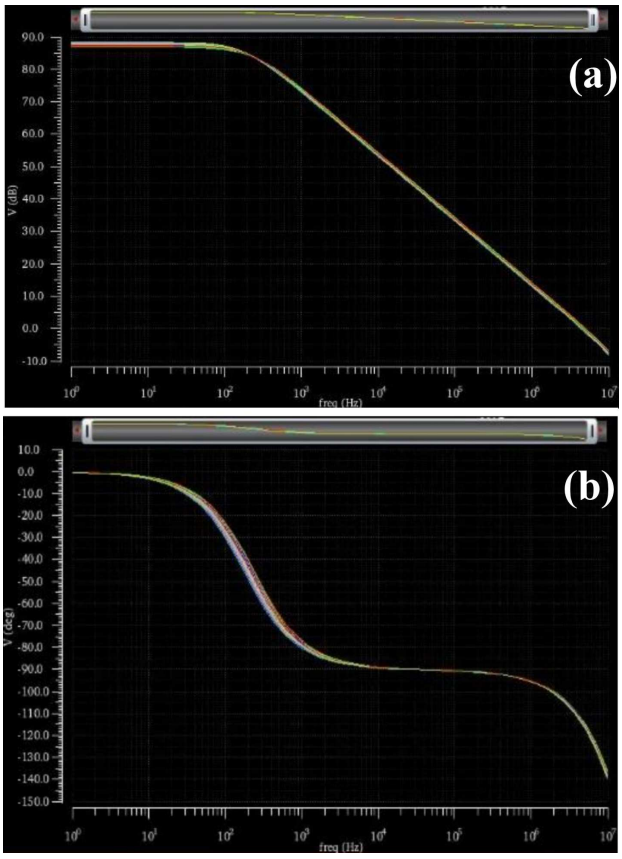

Fig. 3. 45° Corner analysis (a) gain plot and (b) phase plot.

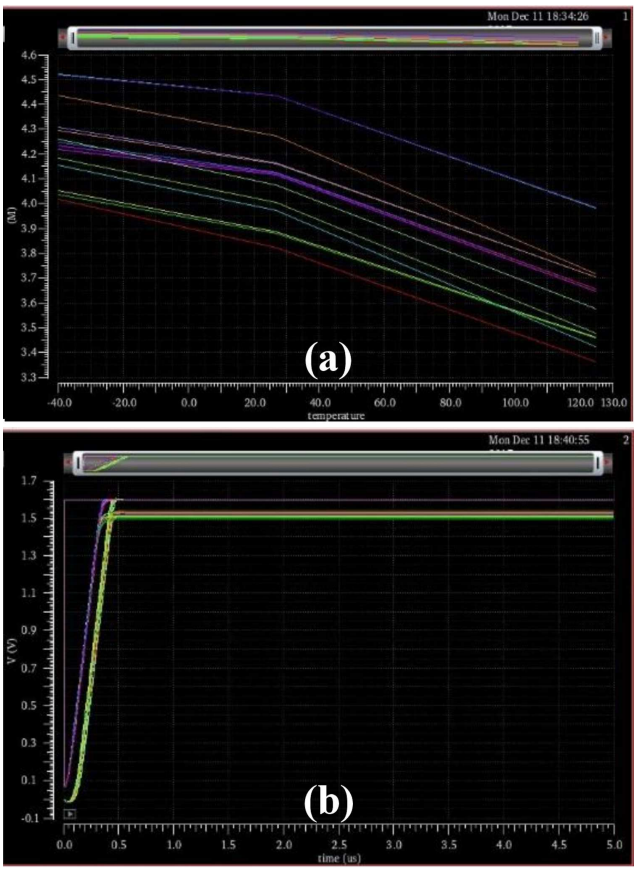

Fig. 4. 45° Corner analysis (a) slew rate and (b) settling time.

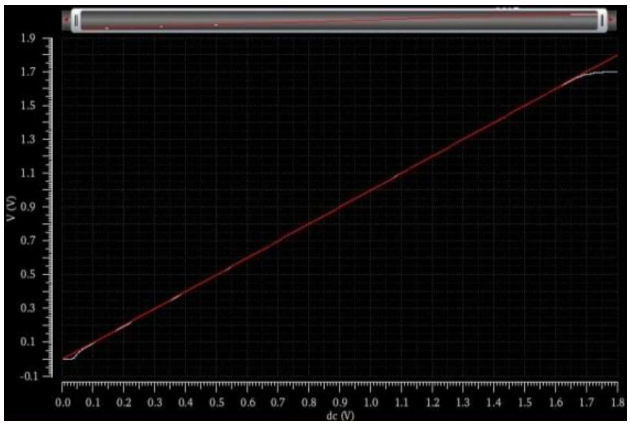

Fig. 5. Input common mode range voltage.

After simulation with SCL parameters, the gain plot is shown in Fig. 3a and the phase plot is shown in Fig. 3b. The slew rate plot is presented in Fig. 4a and the settling time plot is in Fig. 4b. Finally the ICMR plot is in Fig. 5.

From all the plots, the simulated results of the proposed op-amp design values are presented in Table I.

TABLE I

Simulation results of designed op-amp.

S.No.	Parameter	Specifications value	This work	[5]	[6]
1	open loop gain, [dB]	80	87.79	74	67
2	phase margin, [°]	60	67	60	62
3	unity gain frequency, [MHz]	5	4.87	3.68	2.78
4	ICMR range, [V]	0.54–1.26	0.08–1.65	0.09–1.51	0.1–1.47
5	settling time, [μs]	200	339.7	393	521
6	slew rate, [V/μs]	5	4.126	821	190

4. Conclusions

The design of a two-stage op-amp is used for low power and high-speed operations is presented. While simulating at 45° corners, the obtained results are maximum gain is 95.29 dB and the minimum gain is 80.54 dB, and the maximum PM is 70.07° and the minimum PM is 63.36°. The maximum value of slew rate is 4.525 V/μs and minimum slew rate value is 3.48 V/μs. The minimum bandwidth is 3.728 MHz and the maximum bandwidth is 6.067 MHz. The ICMR range is 0.07–1.65 V and the total power dissipated is 75 μW. The Monte-Carlo simulation also done to see the effect of device and process mismatches. The front-end design result shows that the designed circuit is meeting the specification.

Acknowledgments

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