Supplementary Material

Appendix: Scanning CCD Implementation Details

The details of the scanning CCD detector design and implementation are discussed below.

A1. Opto-Mechanical Design

Building on development concepts explored for design of previous CCD cameras that have been built at Argonne laboratory over the years, a novel device was designed to meet the needs for a scanning CCD . A Kodak (Rochester, NY, USA) KAF-16801 CCD was chosen for its small pixel size and large number of pixels (9 μm x 9 μm and 4096 x 4096 pixels) and because all lines of pixels are read from one direction on the chip, rather than in both directions, a requirement for this scanning application. In addition the CCD has a relatively fast line readout of up to a 25MHz pixel rate, allowing all 16M pixels to potentially be read as fast as 2s and when scanning, a single line in less than 1 ms.

To make optimal use of the CCD's fine spatial resolution, a scintillator is needed that does not allow the cone of scintillation photons to bloom (spread) significantly beyond the size of a few pixels. This is accomplished using a Scint-X (Stockholm, Sweden) structured scintillator designed for 20 μm resolution, which is composed of a silicon wafer that is etched with small pockets that are filled with Gd_2S_2O-based phosphor material. This scintillator is bonded to a 1:1 Incom (Charlton, MA, USA) fiber-optic faceplate, which in turn is bonded to the CCD. Bonding is done with optical grease from Nye Lubricants, Inc. (Fairhaven, MA, USA) that fills the gaps between scintillator, faceplate, and CCD, thus reducing intensity loss from reflections. The Scint-X scintillator produced for 20 μm spatial resolution has dimensions of 16 mm by 24 mm, which is only about half the active area of the CCD chip; our prototype used only one scintillator thus sacrificing efficiency for simplicity. The use of a fiber-optic faceplate results in somewhat lower spatial resolution, but simplifies assembly and shields against high energy x-rays directly impinging on the CCD. It should be noted that 1:1 fiber-optic devices are much less expensive than ones that magnify or demagnify.

To minimize cost and weight our entire camera is enclosed in "3-D printed" rapid-prototype plastic case as diagrammed in Figure A1. The CCD is housed in a small plastic housing about 75 mm x 75 mm x 60 mm and cooled with a thermo-electric cooler (TEC). Dry N_2 gas is continually flowed through the housing to keep the CCD free of condensation or ice. A copper heat sink, in the form of a ~25 mm diameter screw threaded through the plastic housing wall, presses the TEC

against the CCD-faceplate assembly to both maintain the optical grease bonds and remove heat from the TEC. A small commercially available fan/heat-sink assembly is mounted on the copper screw outside the housing to remove heat. Optionally, a small water-cooled block could replace the fan and heat-sink for more efficient cooling. To assure the CCD is not cooled without the flow of dry N_2 gas, the housing is pressurized slightly above ambient and is monitored by a small pressure sensor. To provide electrostatic shielding for the CCD the plastic housing is painted inside with conductive paint, while the outside of the housing is painted with black paint to provide light tightness. The x-ray window on the front of the housing is a thin piece of plastic that is simply printed as part of the housing allowing for a one-piece design. The housing is sealed with RTV silicone caulking material to protect camera components against damage from moisture.

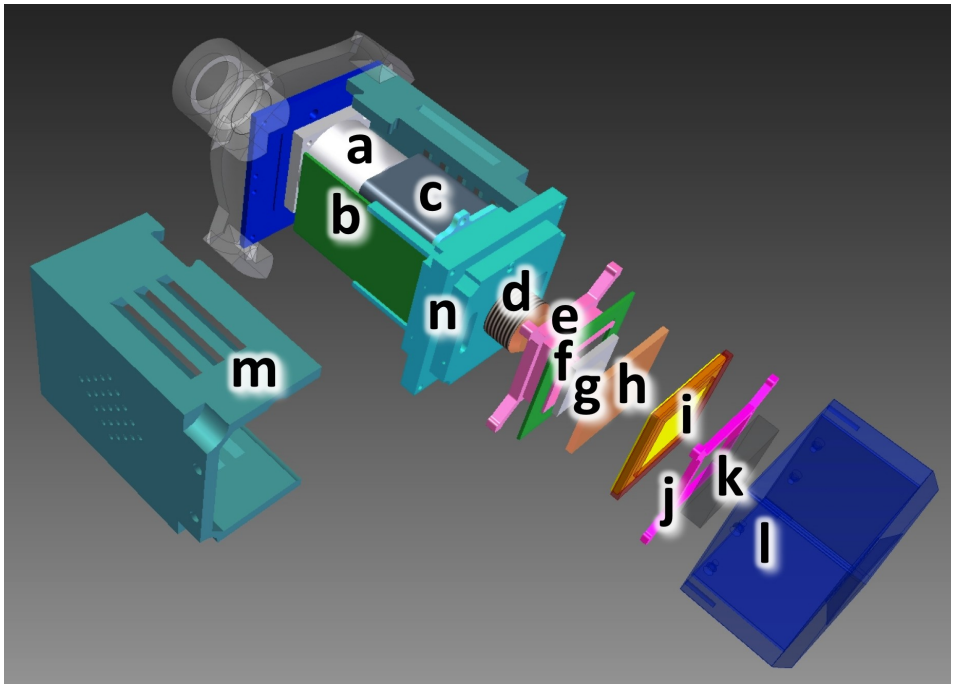

Figure A1: An exploded view of the prototype scanning CCD module. Components

include (a) cool air pipe; (b) circuit board; (c) fan/heat sink; (d) copper heat sink screw; (e) plastic spring; (f) CCD socket circuit board; (g) thermo electric cooler, hot heat spreader; (h) cold heat spreader; (i) CCD, bond wire cover; (j) plastic spring; (k) fibre-optic faceplate; (l) sealing front cover; (m) vented back cover; (n) sealing back cover.

A2 Electronics

A2.1 Circuit Boards

The camera has three main circuit boards: a CCD socket board inside the housing, a credit-card sized board just outside the housing labeled as the "interface board," and a main circuit board which is held in an external case and cabled to the camera head. The CCD socket board is connected by a flex cable that extends through the plastic housing wall and is sealed with RTV. The interface board residing in the camera head, but outside the housing, houses a differential pre-amplifier for the CCD-output and the high speed CCD-clock driver chips for reading out the CCD. A flex cable of ~½ m length connects the interface board and camera head to the main electronics board, but this could be made perhaps two or three times longer with no signal degradation. The CCD data is transferred to a Windows PC for data storage via a Camera Link interface based on a commercial frame grabber card from Teledyne DALSA (Waterloo, ON, Canada). The PC runs the EPICS AreaDetector software to control the camera and store data. The images are recorded from the frame grabber as a series of 4K by 4K images in separate files.

A2.2 Main Circuit Board

The main circuit board is approximately 100 mm x 200 mm in size and houses support electronics for the CCD clock drivers, analog differential receiver and gain stages, an analog-to-digital converter, a FPGA for CCD clock control, digital filtering circuits and a Camera Link interface. Typically in a CCD camera, correlated double sampling (CDS) is employed for low-noise CCD readout . CDS is the process of sampling the output of the CCD after resetting it to a reference voltage, then sampling after signal charge is shifted into the output stage and taking the difference. Historically, CDS was typically done with the combination of an analog switch and analog-to-digital converter. This camera performs CDS digitally through continuously sampling

the CCD output at 60 MHz and performing CDS and averaging in an FPGA. By varying the number of averaged samples, the CCD readout speed can thus be varied to trade off speed for noise performance. Further, the system is simplified because complex analog filters and analog switch need not be included on the board. Due to limitations in our prototype configuration, the line pixel readout rate is limited to 700 Hz rather than the chip limitation of 2 kHz line rate, but we plan to improve this in a future revision.

A2.3 CCD-Motor Synchronization

The CCD is synchronized to the detector motion by triggering the readout of a line after a certain number of motor pulses. Note that we label the ratio of the separation between CCD pixels to the motor step size as F, which must always be less than unity. A 48-bit digital integrator is used with inputs F (as a 32-bit integer) and a pulse for each motor step, as diagrammed in Figure A2. This effectively multiplies the inputs, with results greater than one causing the integrator to overflow. The overflow triggers the reading of a single CCD line. Note that since the integrator value retains the portion of the value after dropping one, this implementation successfully synchronizes the detector arm and detector readout, even when there is not an integral relationship between motor pulses and the pixel size (where F is not the ratio of integers.)

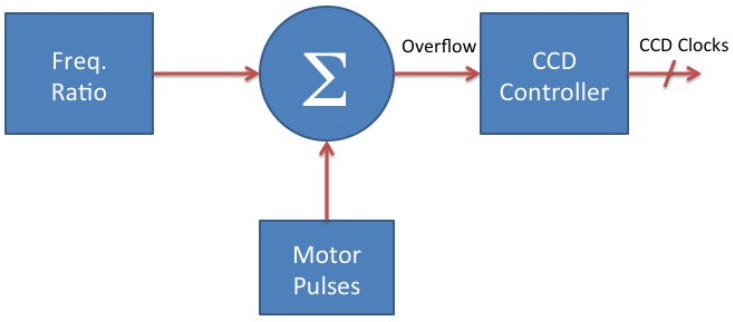

Figure A2: A schematic diagram of the integration circuit that links the motor pulse signal to the scanning of individual CCD lines.

A3 Specifications

The measured specifications of the camera and electronics are reported as Table 1 in the main article. The gain was measured by flooding the CCD with visible light and using the average light level over several exposures and photon Poisson noise . Read noise was measured by simply reading out the final horizontal shift register without vertically shifting the lines, thus removing dark current and fixed pattern noise. Dark current was measured by taking several exposures at varying time lengths at room temperature and using the dark current doubling temperature listed in the CCD datasheet from Kodak. The full well capacity, i.e. the maximum amount of charge that can be held in a pixel before smearing to adjacent pixels occurs, was measured by taking long dark exposures and noting the maximum signal level in isolated pixels. The spatial resolution was measured by putting a knife-edge at the detector front and exposing with an x-ray tube. We determine the line response of the detector by fitting a sigmoid function to the observed image at the shadow of the knife-edge. We differentiate this sigmoid function to estimate the point spread function.

References

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