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An Ultra Low Power Space Application based Radiation-Hardened Low Voltage 4T SRAM Bitcell

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Abstract: ***Continues transistor scaling, exacerbates the situation, as susceptibility to soft-errors is increased in VLSI circuits, particularly when exposed to severe environmental conditions, such as cosmic radiation and charged particles .Silicon covers most of the area in the memory arrays and regularly stores the basic information.***
Radiation solidifying of inserted memory arrays is normally accomplished by actualizing incredibly expansive bit cells and keeping up a moderately high operating voltage; however, in addition to the resulting area overhead, this often limits the minimum operating voltage of the entire system leading to significant power consumption.In this paper, we propose a radiation-solidified static random access memory (SRAM) bitcell focused at low-voltage usefulness, while keeping up high soft-error robustness.
The proposed 4T SRAM bit cell have a novel dual-driven seperated feedback mechanism to achieve high soft-error tolerance robust operation down to 300 mV.
Index Terms: Low voltage, radiation effects, radiation soldifying, single-event upset (SEU), soft errors, space applications, static random access memory (SRAM), subthreshold, ultralow power (ULP).

I. INTRODUCTION

Power dissipation is one of the most dominant aspects of current nanoscale VLSI circuits.Ultra low power (ULP) operation is increasingly in demand for future System-on-Chip (SOC) circuits for space applications, where energy resources are limited.
Future little, minimal effort satellites have an even lower control financial plan, as the all out satellite weight is regularly diminished by limiting the utilization of substantial batteries and power supplies.
The most proficient approach to accomplish ULP operation in incorporated circuits is to forcefully diminish the supply voltage (VDD) what's more, work all segments of the chip near or on the or on subthreshold region [1], [2], in this way fundamentally diminishing both static and dynamic power utilization.
The supply voltage can be reduced to the deep sub-threshold region, dramatically saving power in logic and memory. Extremely low-power design was first explored in the 1970s for the design of applications such as wristwatch and calculator circuits. [3].
Soft errors or single-event upsets (SEUs) occurred by radiation strikes are the essential causes of failures in VLSI circuits working in a hard radiating environment.
Package radioactive decay usually causes a soft error by alpha particle emission. The positive charged alpha particle travels through the semiconductor and disturbs the distribution of electrons there. If the disturbance is large enough, a digital signal can change from a 0 to a 1 or vice versa.
In combinational logic, this effect is transient, perhaps lasting a fraction of a nanosecond, and this has led to the challenge of soft errors in combinational logic mostly going unnoticed. In sequential logic such as latches and RAM, even this transient upset can become stored for an indefinite time, to be read out later. Thus, designers are usually much more aware of the problem in storage circuits.
The contributions of this paper are as follows.

1) The proposed radiation-hardened bitcell is a pioneer solution for embedded memories in low-power space applications.
2) Implementation of SRAM arrays based on the proposed bitcell reduces area and power consumption.
3) The proposed solution shows an outstanding advantage over the conventional 6T SRAM cell.
4) High-radiation tolerance is achieved under scaled supply voltages, into the subthreshold region.
5) In order to improve the bitcell robustness, a novel dual-driven separated-feedback mechanism is introduced and implemented.

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II. STANDARD SRAM UNDER SEUs

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations.In addition to such six-transistor (6T)SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit.[4],[5],[6].Four-transistor SRAM is quite common in stand-alone SRAM devices(as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors[7].Four transistor SRAM provides advantages in density at the cost of manufacturing complexity.The resistors must have small dimensions and large values.This sometimes used to implement more than one(read and or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry.

Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing a silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory.Memory cells that use fewer than four transistors are possible – but, such 3T or 1T cells are DRAM, not SRAM (even the so-called 1T-SRAM).Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs – in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down.

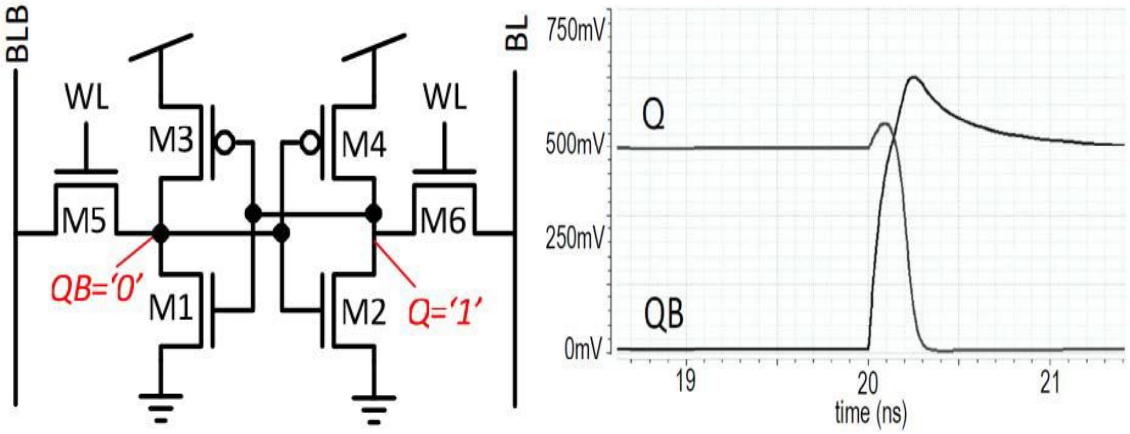

Fig. 1. (a) Standard 6T SRAM bit cell. (b) Example of an SRAM bit flip caused by an SEU.

III. PROPOSED 4T RADIATION TOLERANT BITCELL

SRAM design for low-voltage operation has turned out to be progressively mainstream in the recent past.Different bitcell designs and building procedures have been proposed to enable operation profound into the subthreshold region [15].These designs commonly join various transistors into the bitcell topology,contrasted with the standard 6T SRAM bitcell,exchanging off thickness with strong, low-voltage functionality. Be that as it may, these bitcells were intended for activity under standard working environments,and in this manner, don't give adequate power to SEUs under high-radiation conditions. What's more, the plan engineering of these phones depends on the standard 6T cell;therefore, the 6T cell has a similar solidifying capacity to most, if not all, these unprotected cells. As the radiation solidifying capacity of the 6T cell is amazingly low, particularly when contrasted and radiation solidifying arrangement structures radiation hardening solution designs.

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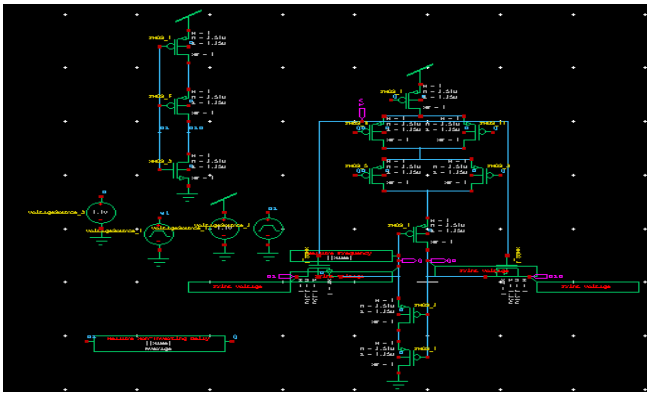

Fig. 2. Schematic of the proposed 4T radiation-hardened bitcell.

The schematic representation of the proposed 4T bitcell is shown in Fig. 2.The storage mechanism of this circuit comprises separate nodes with the acute data value stored at its center Q . This node is driven by a pair of CMOS inverters made up of transistors that are, respectively, driven by the inverted data level,stored at *Q* respectively,driven to *V*DD or GND through devices P1, P2, N1, and N2 that are controlled by the weak feedback nodes that are connected to *Q* through a pair of complementary devices .By driving the acute data level by a pair of equipotentially driven,yet independent, inverters, a strong, dual-driven feedback mechanism is applied with node separation for the protection of circuits from SEU. While achieving a high critical charge at node *Q* this setup effectively protects *Q* from an upset.The proposed 4T bitcell highlights two stable states, speaking to a rationale 1 and a rationale 0, characterized as the voltage level at hub Q.Comparable to a standard cross-coupled inverter structure, reversed voltage levels are held at the inward information hubs.

Two basic principles provide the proposed bitcell with inherent SEU tolerance.

1) The data are read out from node Q, such that any temporary upset on different nodes can be endured.

2) The assisting nodes are designed with redundancy to ensure that any upset will be moderated by the other nodes

Standard SRAM topologies, such as the 6T bitcell,write data by driving the new level directly into the storage nodes, and therefore are required to overcome the circuit's strong internal feedback.But the proposed 4t sram bitcell achieves writes by driving the weak feedback nodes, thereby removing much of the ratioed contention, inherent to direct access. A pair of write access transistors connect a unified write bitline (WBL) to the weak feedback nodes. These devices are controlled by a write word line (WWL), such that when WWL is raised,they are pulled toward the level driven upon WBL.

IV. SEU TOLERANCE

A. Disrupt Modeling

This paper proposed a 4T SRAM bitcell, designed for robust,upset tolerant, low-voltage, ULP operation in high-radiation environments,such as those encountered by space applications. At the point when a particle strike, the normal for such a situation, goes through a semiconductor material, a disturb happens because of the drift current of the created e–h pairs in a reverse biased p-n junction.If the molecule hits an unbiased junction, the produced e–h pairs will spontaniously recombine and not actuate a current because of the absence of an electric field. However,a strike on a reverse-biased junction causes a transient current [*I (t)*] at the connected node, characterized by a fast rise time and a gradual fall time. This current can be

$$I(t) = \frac{Q_{\text{coll}}}{t_f - t_r}\left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}}\right) \qquad (1)$$

where *Q*coll is the charge collected due to the particle strike, *tf* is the fall time and *tr* is the rise time. *Q*coll depends on the type of the ionizing particle,trajectory,energy value,and impact location.

B. Disrupt Tolerance

The different internal nodes of the proposed 4T bitcell and the likelihood of strikes of both positive and negative polarities require an investigation of each kind of strike to assess upset tolerance.The correct readout just requires the information to be steady at node Q, and consequently, it is adequate to consider the voltage at this node for such an assessment.

V. SIMULATION RESULT

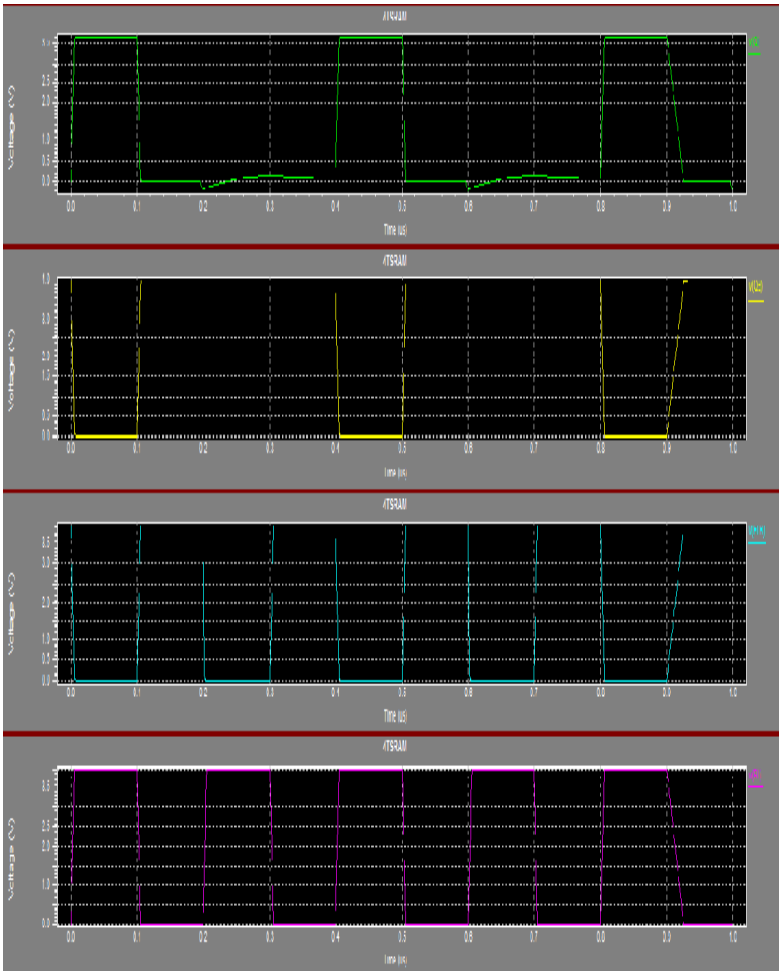

Fig.10 Simulated waveform for 4T SRAM bitcell in Tanner EDA

VI. CONCLUSION

This paper proposed a 4T SRAM bitcell, intended for hearty, low-voltage, ULP activity in high-radiation conditions,for example, those experienced by space applications.

TABLE 1
AVERAGE POWER CONSUMPTION

SRAM CELL	POWER
13T	2.64mw
11T	0.0106 mw
5T	0.233mw
4T	7.4uw

This paper proposed a 4T SRAM bitcell, designed for robust, low-voltage, ULP operation in high-radiation environments,such as those encountered by space applications.The proposed circuit displays a novel dual-driven separated feedback mechanism to achieve high soft-error tolerance robust operation down to 300 mV.

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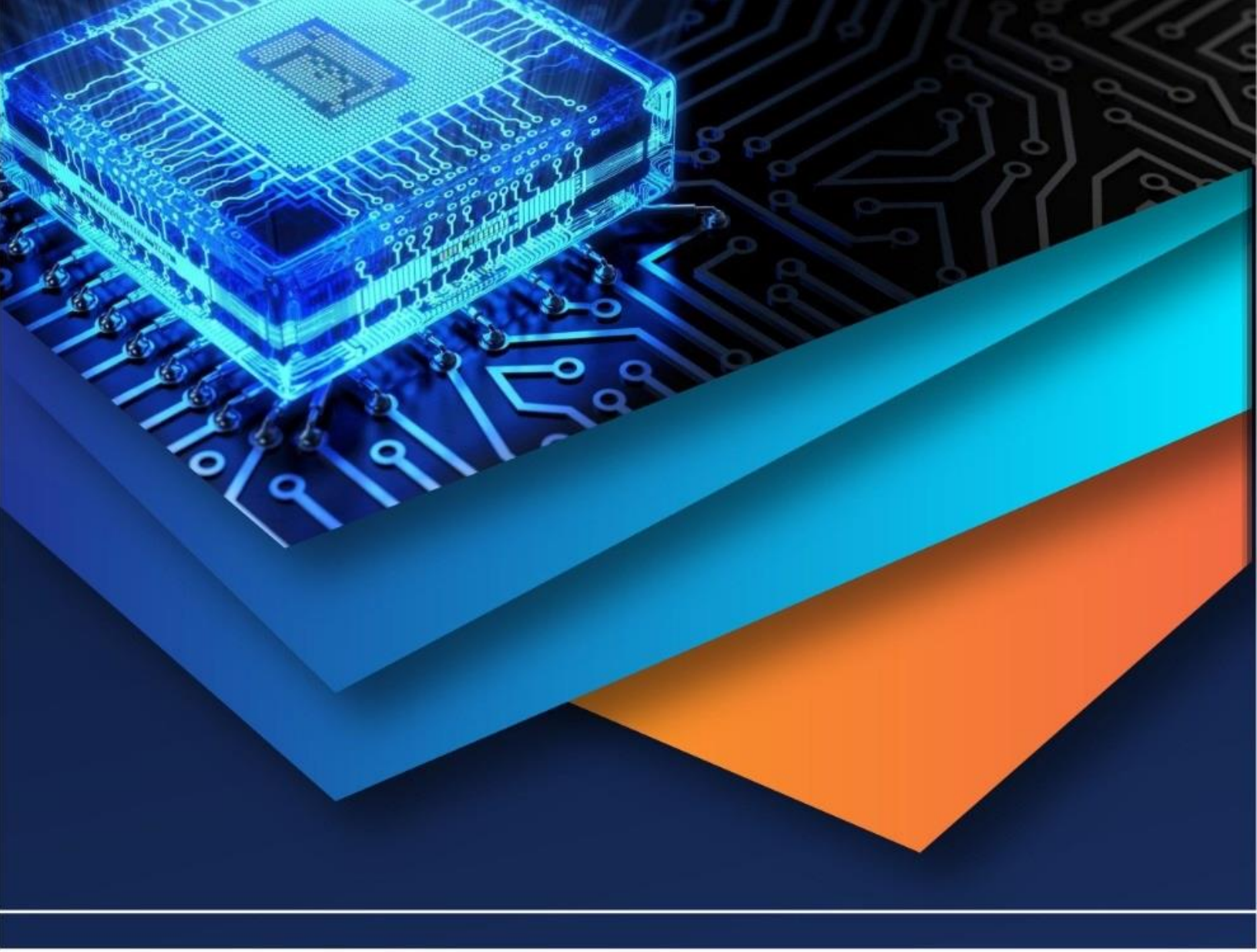

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