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Design and Implementation of a Low Power Vedic Multiplier

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Abstract: ***This paper proposes the design of a low power Vedic Multiplier using the technique of Vedic Mathematics that has been modified to reduce the power consumption.Vedic multiplier is based on a novel concept in which the partial products are generated using concurrent additions. In this paper an 8 bit Vedic multiplier is designed using four 4 bit Vedic multipliers and various adder circuits. The adder circuits are realized using mux based adders instead of conventional adders as in normal Vedic multipliers. The 8×8 Vedic Multiplier circuit is coded in verilog, synthesized and simulated using Cadence Software. The power consumption and area of the multiplier using MUX based adders are compared with existing ones. Results show that the power consumption is reduced by 41% when compared to conventional Vedic multipliers and the results appear to be promising. The combination of low power and lesser area makes the new multiplier a viable option for implementing low power designs.***
Keywords: Vedic Multiplier, Urdhava Tiryakbhyam sutra, low power , Digital signal processing, MUX Based adder

I. INTRODUCTION

To develop low power and area efficient portable electronic design is a very challenging in the current scenario. The significance of the digital computing lies in the multiplier design. Recent developments in processor designs mainly use low power multiplier architectures. The multipliers play a significant role in arithmetic operations in various DSP applications. Two significant and often conflicting design criteria are power consumption and speed. Taking into consideration of these constraints, the design of low power multiplier is of great interest in DSP processors, portable consumer electronic products such as smart cards, assistive listening technologies like hearing aids and PDAs. The main concerns of these products are not only the computational capacity but also to extend the operating hours of the battery within it. Different Vedic multipliers [1-5] are discussed in the literature. These Vedic multipliers are implemented using conventional full adders such as Ripple Carry Adder (RCA) and Carry Select Adder (CSA). This paper proposes a novel low power 8x8 Vedic multiplier design using MUX based adder circuits for low power applications. The rest of the paper is organized as follows. Section A gives the introduction to the Vedic Mathematics and the principle of multiplication. The existing multipliers are discussed in section II. Section III deals with the proposed multiplier architecture. The results are shown in section IV and finally the conclusion is summarized in section V.

A. Vedic Mathematics And Urdhva-Tiryakbyham Sutra

Veda is a Sanskrit word which means ‘Knowledge’. Vedic Mathematics is a collection of techniques or Sutras to solve mathematics in a easy and faster way. It consists of 16 Sutras which can be used for problems involved in arithmetic, algebra, geometry, calculus, etc. Urdhva Tiryagbhyam is the most generalised sutra for implementation of Vedic multiplier designs. The beauty of Vedic Multiplier lies in the fact that they can be used to solve cumbersome mathematical operations and thereby improving speed. It literally means “Vertically and crosswise” where the partial products are generated simultaneously. The multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

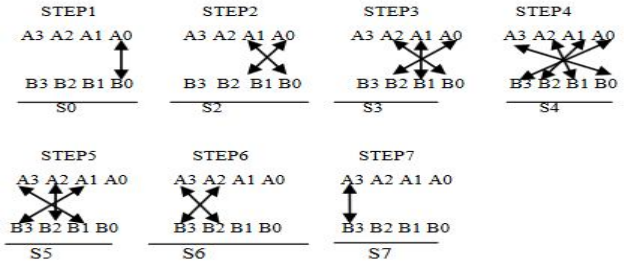

Figure 1: Vertical & Crosswise Technique

Consider two 4-bit binary numbers A3A2A1A0 and B3B2B1B0. The partial products and their sums are calculated in parallel by using the following equations:

Step1: S0 = A0*B0
Step2: S1 = A1*B0+A0*B1
Step3:S2= A2*B0+A0*B2+A1*B1
Step4:S3= A3*B0+A0*B3+A2*B1+A1*B2
Step5:S4= A3*B1+A1*B3+A2*B2
Step6:S5= A3*B2+A2*B3
Step7:S6= A3*B3
The final output is: S0S1S2S3S4S5S6

II. EXISTING ARCHITECTURES

A. 4-Bit Vedic Multiplier

Fig. 2 shows the architecture of 4x4 Vedic multiplier. The multiplier uses 9 full adders and 4-bit special adder. The 4-bit special adder is used to reduce the delay of multiplier. Full adders are implemented using basic gates as shown in Fig.3. Fig. 4 shows the 4-bit special adder [6].

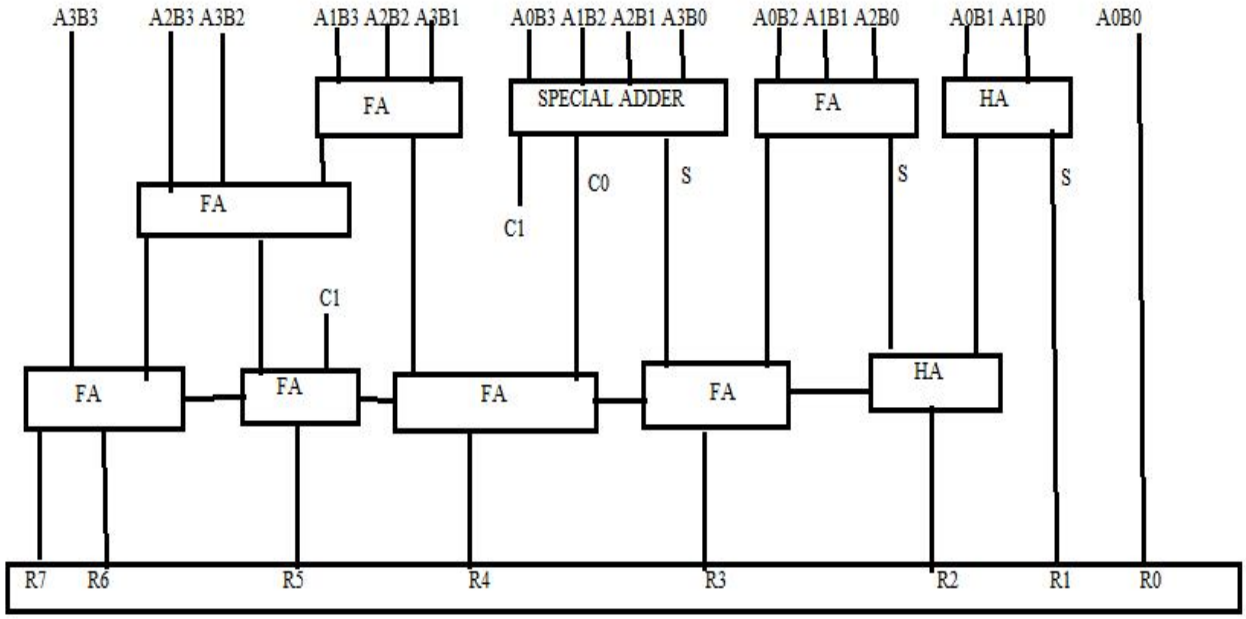

Fig. 2: 4-bit Vedic multiplier.

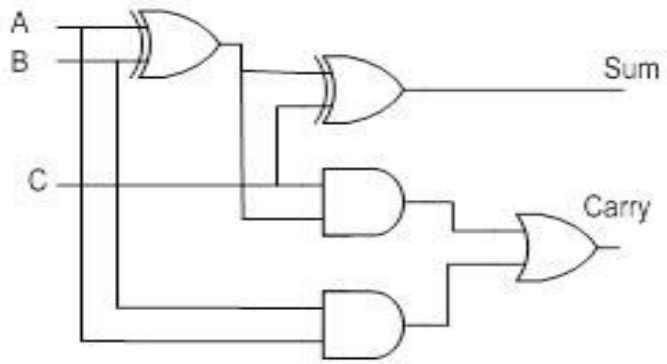

Fig. 3: Conventional 1-bit Full Adder

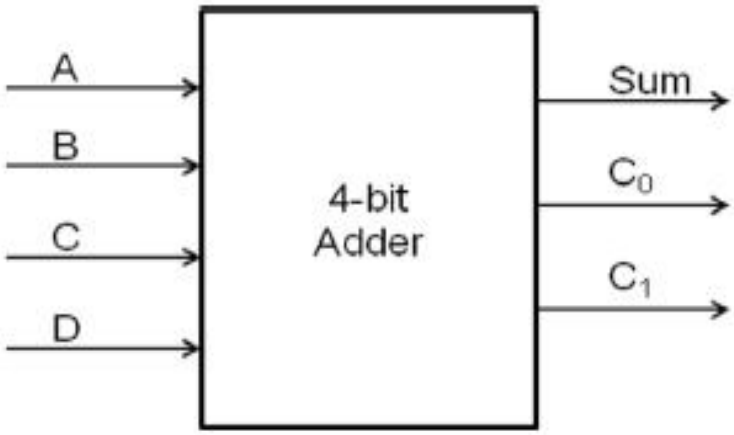

Fig.4: Structure of 4-Bit special adder

The special adder is used in the multiplier to improve the speed of the design. Let A, B, C, D be the four inputs. C0 and C1 are LSB and MSB of carry outputs respectively and Sum is the sum of four inputs.
The Boolean expressions for the sum and carry are given below.
Sum= A XOR B XOR C XOR D
C_0 = ((NOT B) AND D) OR (C AND (NOT D)) OR (B AND (NOT C))
C_1 = A AND B AND C AND D

B. 8x8 Vedic Multiplier Using RCA

Fig 5 shows the 8x8 Vedic multiplier using RCAs. The multiplier uses four 4x4 multipliers and 3 RCAs[6]. The RCA uses the conventional full adders using basic gates.

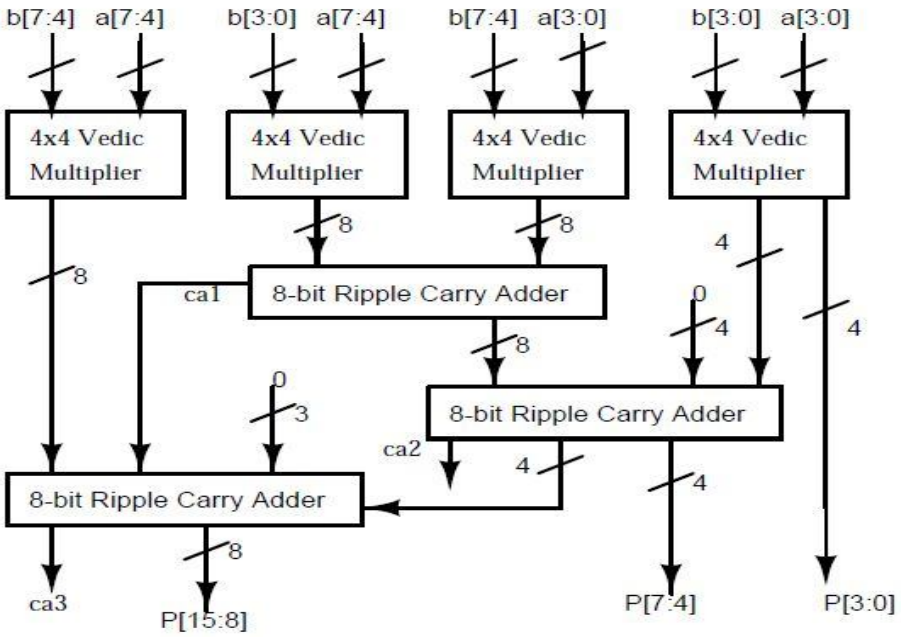

Fig. 5: 8x8 Multiplier using Ripple Carry Adder

C. 8x8 Vedic Multiplier Using CSA

Fig 6 shows the 8x8 Vedic multiplier using CSAs. The multiplier uses four 4x4 Vedic multipliers and 3 CSAs. As the CSA has less delay compared to that of the RCA, multipliers using CSAs are used in high speed applications [7].

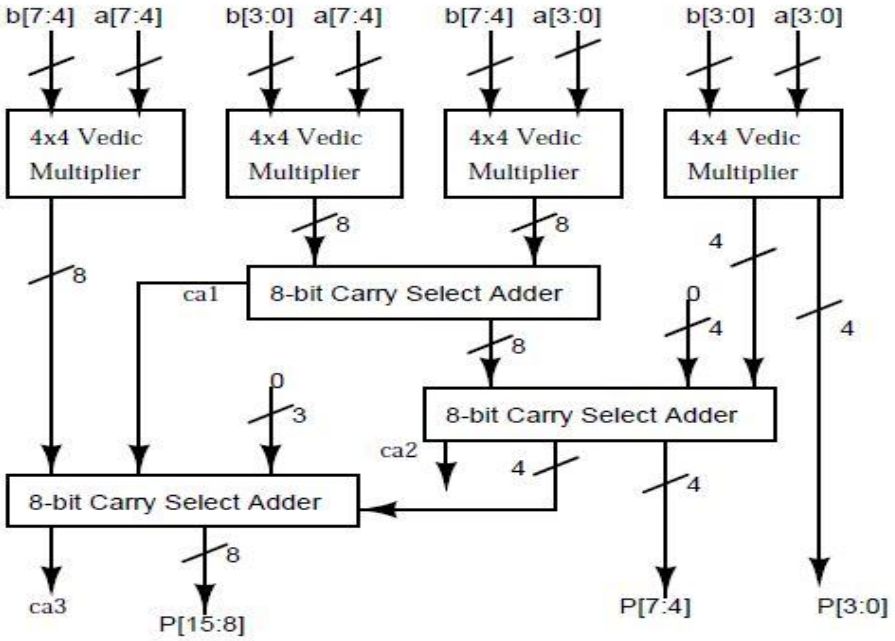

Fig. 6: 8x8 Multiplier using Carry Select Adder

III. PROPOSED 8X8 VEDIC MULTIPLIER

The proposed 8x8 Vedic multiplier is shown in Fig.7.

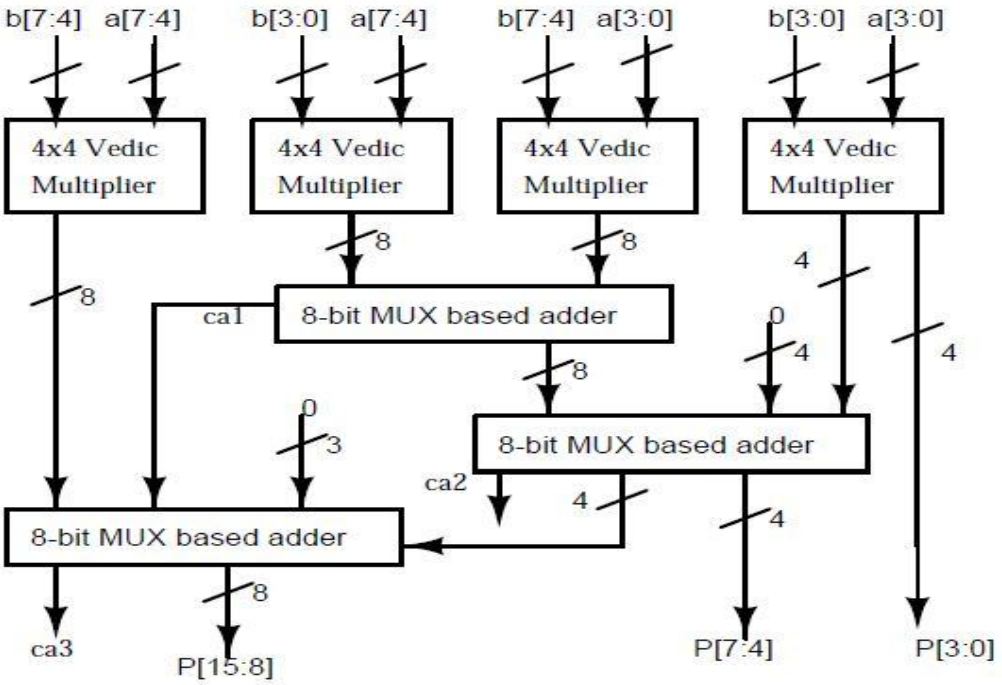

Fig.7: Architecture of proposed 8×8 Vedic Multiplier

The conventional full adder consists of two XOR gates in critical path of sum and one XOR gate, one AND gate and one OR gate in the critical path of the carry. The bottleneck of full adder is high power consumption due to XOR gates. Therefore to reduce the power and area, all the conventional adders are replaced by MUX based adder circuits in the proposed design. The structure of a MUX based full adder is shown in Fig.8. In this, the full adder is implemented using two 2:1 MUX and an XOR gate.

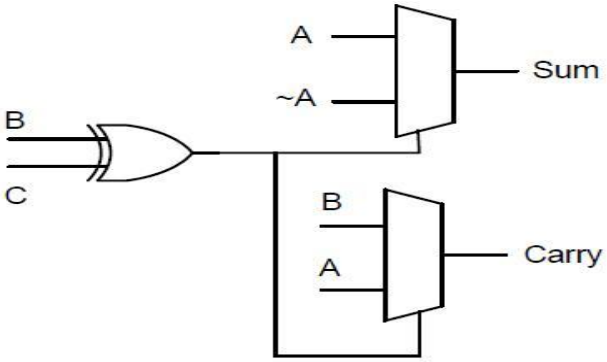

Fig.8: Structure of the MUX based full adder

IV. RESULT AND DISCUSSIONS

The proposed 8-bit multiplier is coded in Verilog HDL, simulated using Cadence NC simulator, synthesized using Cadence's RC encounter and verified for all possible inputs. The simulation inputs are generated using suitable Verilog test bench.

A. Simulation and Synthesis Output

The simulation result for 8-bit multiplier is shown in Fig. 9 and the synthesized schematic is shown in Fig. 10.

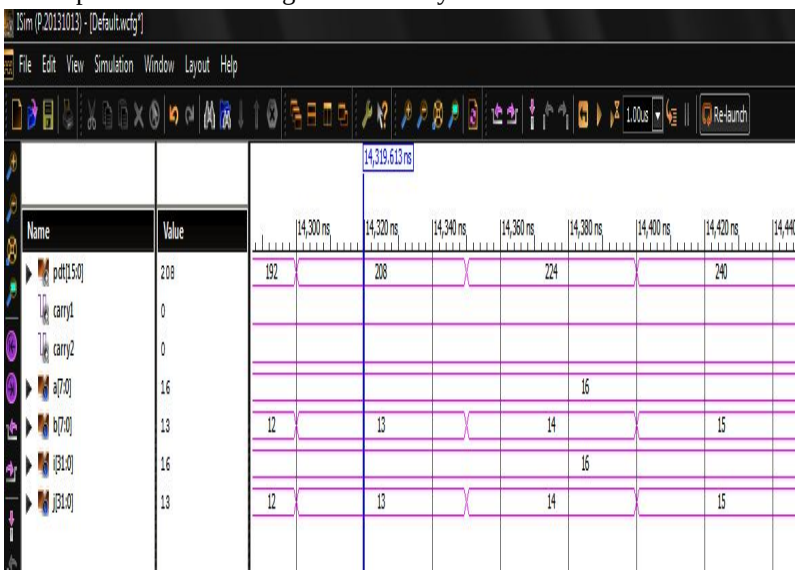

Fig .9: Simulation result of Proposed 8*8 Multiplier

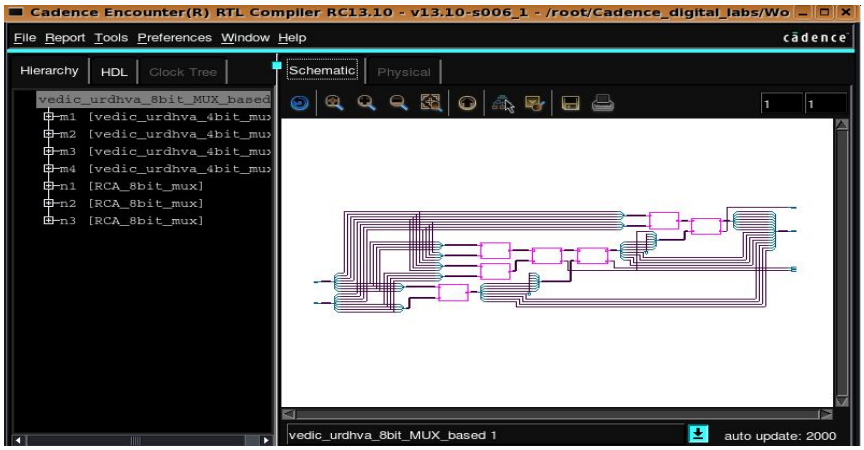

Fig.10 : Synthesized schematic of Proposed 8*8 Multiplier

B. Results And Comparison With Existing Architecture

The 8-bit MUX based adder designed is compared with the ripple carry adder and carry select adder in terms of total area and power. The results obtained are tabulated in table I. From table 1, it is evident that there is a substantial reduction in the parameters.

Table 1: Comparison Of Various 8 Bit Adder Circuits

Adders	Ripple Carry Adder	Carry Select Adder	MUX Based Adder
Area (In terms of cells)	336	610	216
Power (µW)	7.15	12	6.5

The 8*8 multiplier is then designed using the MUX based adder and is compared with the existing designs using ripple carry adder and carry select adder and the results obtained are tabulated in Table 2. Results show that the Vedic multiplier using MUX based adders consumes 50.54 µW of power. Hence power dissipation is reduced by 41% compared to the multiplier using CSAs and 14 % compared to that of using RCAs. Results also shows that the proposed multiplier consumes less cell area compared to the existing architectures.

Table 2: Comparison Of 8 Bit Vedic Multipliers Using Different Adders

Vedic Multipliers	Using RCA	Using CSA	Using MUX based adder
Area (In terms of cells)	2787	3607	1850
Power (µW)	64.23	86.15	50.54

From table 2, it can be seen that the area and power consumption using MUX based multiplier is less compared to other Vedic multipliers. Also the performance of Vedic multiplier is high compared to array multiplier or other multiplier architectures [8-10]. Hence it can be very much suitable for area and power critical designs.

V. CONCLUSIONS

This paper presents a multiplication "Urdhva Tiryakbhyam" Sutra based on Vedic Mathematics and a design of the 8x8 bit Vedic multiplier using MUX based adders. The paper describes a method to reduce area and power consumption by using MUX based addition technique. The design is implemented using Cadence and the results show less area requirement and low power consumption. The work can further be extended to 16x16, 32x32 multipliers and their comparisons can be studied. The proposed architecture can be used to develop a compact, low power multiplier in arithmetic applications.

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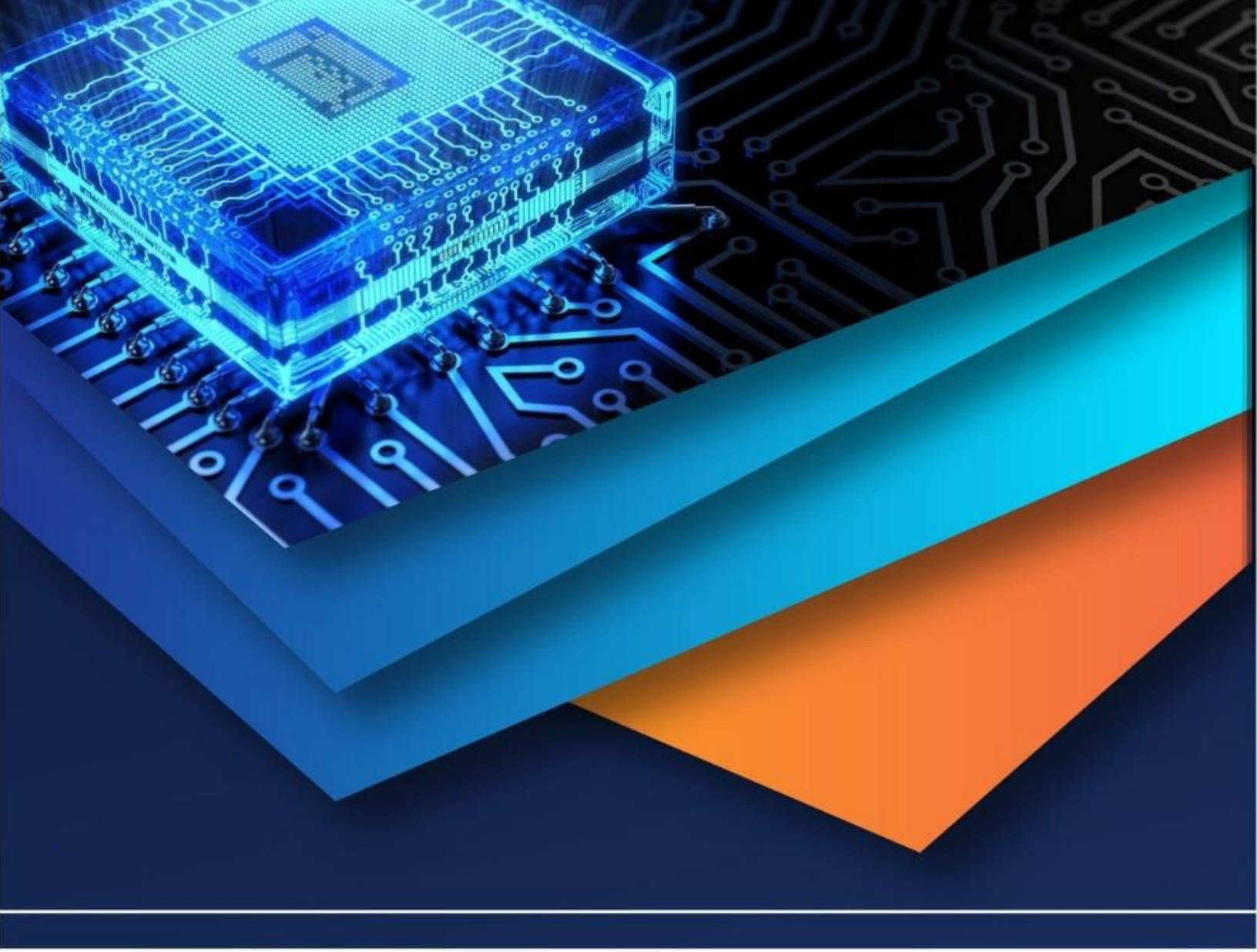

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