# DESIGN AND ANALYSIS OF A LOW POWER BOOTSTRAPPED CMOS CIRCUIT

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## Abstract

*This paper describes bootstrapped circuit operated at low voltage. First I have described bootstrapped driver circuit that operated at ultra low supply voltage. Bootstrapping is a technique that improves the driving ability of digital circuit that operated on very low voltage. In this paper I have proposed bootstrapped driver circuit using CADENCE virtuoso at 180nm as well as 90nm and comparison of both circuit are mentioned and also layout of proposed bootstrapped driver circuit is also shown. The proposed bootstrapped driver circuit minimizes area overhead as compared to conventional bootstrapped driver circuit. Proposed driver circuit uses less number of transistors as compared to conventional driver circuit. Conventional bootstrapped driver circuit operated at 1v to 1.5v, if we try to reduce that supply voltage for low power application then actual working of driver circuit get disturbed at 180nm. The circuit which I have proposed at 180nm takes minimum supply voltage of 0.8v and proposed driver circuit at 90nm take minimum supply voltage of 0.3v. Final output voltage of bootstrapped driver circuit will be boosted output that is above VDD and below GND. Both proposed bootstrapped driver circuit give low power dissipation and less leakage current and also less delay as compared to conventional bootstrapped driver circuit. Proposed bootstrapped driver circuit offers 94.93% improvement in power dissipation.*

***Keywords:*** *Ultra Low Voltage, CMOS Driver, Bootstrapped Drivers.*

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## 1. INTRODUCTION

Nowadays low power supply voltage is the trend of CMOS VLSI digital circuits [1] [2]. Since the threshold voltage of the CMOS devices cannot be scaled down accordingly with the power supply voltage. Minimum threshold voltage cannot scale down beyond defined limit for a standard cell library. Body biasing is another option but it needs extra supply voltage to body terminal. So, designing a CMOS circuit using a low power supply voltage for SOC applications has been challenging. In this paper design of low supply driver circuit has been explored. As we know the design of the driver circuit is the major step in determining the speed performance of a CMOS VLSI circuit with a large capacitive load. To raise and to lower the gate voltage of the output NMOS and PMOS device indirect bootstrap techniques is mainly used in the large load driver circuit using a low power supply voltage [3-5]. In indirect bootstrap technique, the bootstrap technique is applied at the gate of the output devices in a driver circuit. But when the bootstrap technique is applied at gate of the output device it is not effective in shortening the switching speed of the output. Since threshold voltage cannot be reduced with reduction in power supply in CMOS devices and the design of large load driver circuit is with reduced power supply is challenging.

The structure of this paper is as follows: Section 2 gives the scope of study, section 3 show conventional bootstrapped CMOS driver circuit, Section 4 shows design and implementation of proposed bootstrapped driver circuit, Section 5 shows the layout of proposed bootstrapped driver circuit, Section 6 shows post layout simulation results, section 7 will give results and discussion, section 8 gives conclusion of this whole study and at last references given.

## 2. SCOPE OF THE STUDY

The conventional bootstrapped driver circuit cannot work below supply voltage of 1v. If we try to reduce that supply voltage in conventional bootstrapped driver circuit below 1v, then actual working of driver circuit get disturbed. Moreover conventional bootstrapped driver uses more number of transistors that increases overall area of the circuit. The conventional bootstrapped driver uses bootstrap capacitor of large value that in turn increases area and power dissipation of the circuit.

To overcome the problem that occurs in conventional bootstrapped driver circuit I have modified that driver circuit. In conventional bootstrapped driver circuit value of bootstrapped capacitors are very large that is Cp = 350fF and Cn = 250fF, whereas in proposed bootstrapped driver circuit value of bootstrapped capacitors are Cp = Cn = 17fF. In conventional bootstrapped driver circuit when supply voltage Vin = 1v, then output positive level is boosted to Vout = 1.0001v. Whereas in proposed bootstrapped driver circuit when supply voltage Vin = 1v, then output positive level is boosted to Vout = 1.4v. Moreover in conventional bootstrapped driver circuit the number of transistors used is more as compared to proposed bootstrapped driver circuit. So, less usage of transistors leads to reduction in area coverage. I have designed driver circuit using CADENCE virtuoso tool at 180nm as well as 90nm technology. The proposed bootstrapped driver circuit at 180nm technology

takes minimum supply voltage of 0.8v and boost output positive level to 1.17v. The proposed bootstrapped driver circuit which I have designed at 90nm technology takes minimum supply voltage of 0.3v and boosts the output positive level to 0.599v approximately double to VDD.

## 3. CONVENTIONAL BOOTSRAPPED CMOS DRIVER

Figure 1 below shows the circuit of conventional bootstrapped driver, which composed of fundamental segment and bootstrapped segment. In fundamental segment two PMOS devices are used that are PM0 and PM1 and two NMOS devices are used that are NM0 and NM1. In bootstrapped segment two PMOS device that are PM2 and PM3 and two NMOS devices are used that are NM2 and NM3. Transistors of inverter PM4 and NM4 and bootstrapped capacitors C0 and C1 are also included in bootstrapped segment. Here transistors NM2, NM3 and bootstrapped capacitor C0 are used for pull up transient operation, whereas transistor PM2, PM3 and bootstrap capacitor C1 are used for pull down transient operation.

In this circuit it is clear that bootstrap circuit is composed of two portions for pull-up and pull-down operations. Capacitor Cp and NMOS devices N1b/N2b are used for the bootstrapped pull-up operation and capacitor Cn and PMOS devices P1b/P2b are used for the bootstrapped pull-down operation.

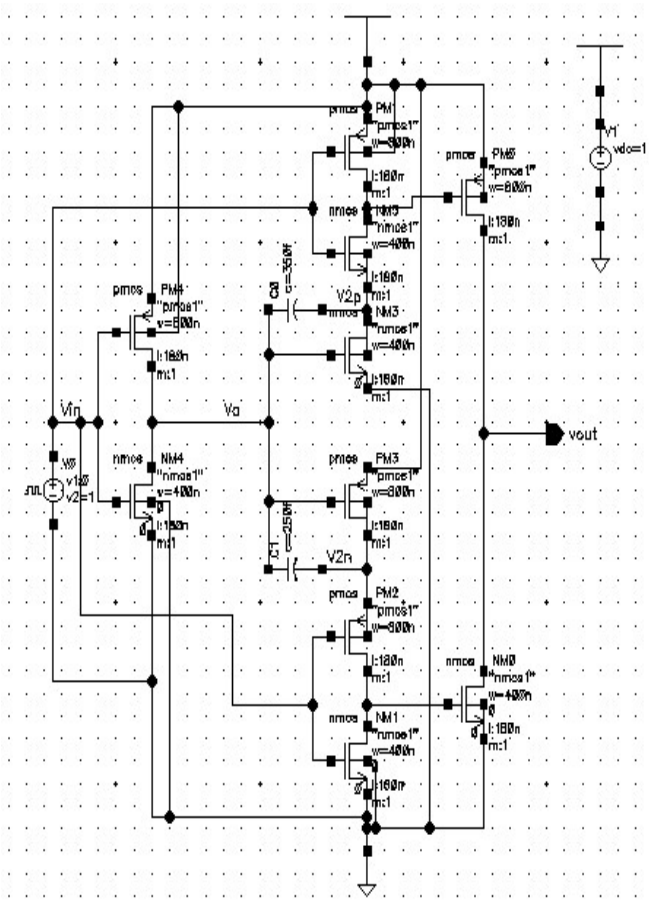


**Fig-1:** Conventional bootstrapped driver circuit

Figure 2 shows the transient waveforms of conventional bootstrapped driver circuit. As shown in figure 1 right side of bootstrapped capacitor C0 or node V2p can go below 0v during the transient.

During pull up transient operation, the operation of this conventional bootstrapped driver circuit is divided into two periods regarding bootstrapped capacitor C0. First is charge build up period and second is bootstrapped period.

From figure 1 when input will get ON. The output of conventional bootstrapped driver Vout, which is indirectly driven by given to this circuit is Vin = 0v, then output of inverter will be 1v which will make transistor NM2 and NM1 get OFF, transistor NM3 PM2 in the bootstrapped segment is 0v.

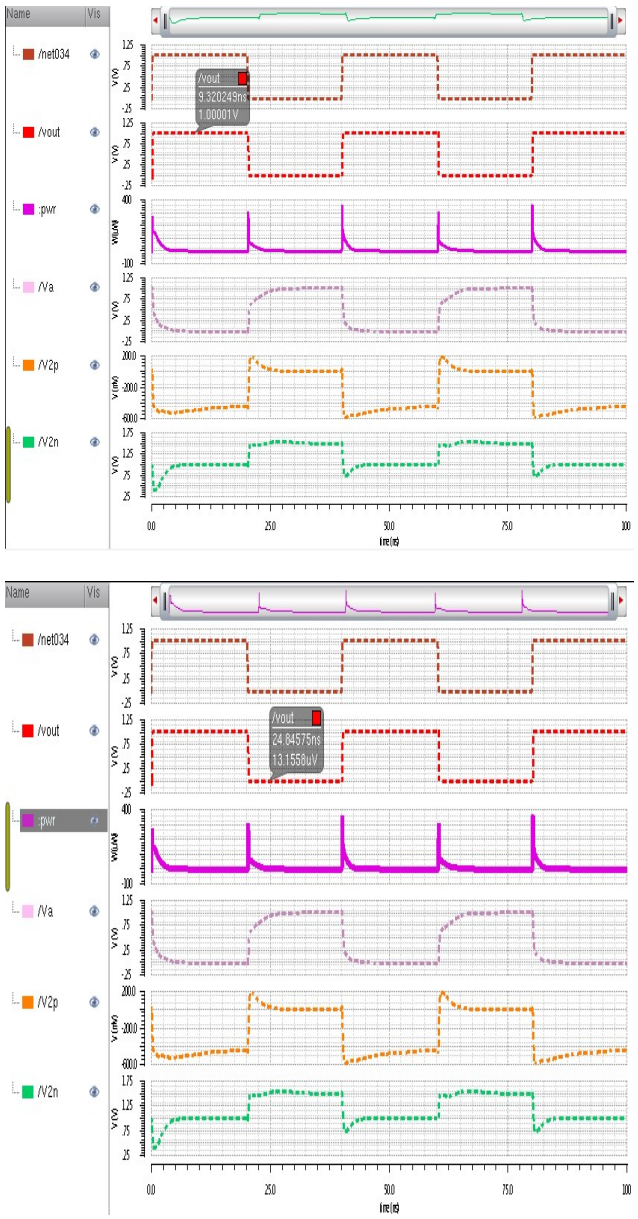


**Fig-2:** Waveform of conventional bootstrapped driver circuit

On the other hand, transistor NM3 and bootstrapped capacitor C0 of bootstrapped segment are separated from the transistor PM1 and PM0 of fundamental segment. As a result the bootstrapped capacitor C0 has charge of 1C0 coulomb, since left side is pulled to 1v and right side is node V2p to 0v because NM3 is ON.

Now when supply voltage given Vin = 1v, the output of inverter Va changes to 0.001v. Due to which right side of bootstrapped capacitor C0 is disconnected from GND because transistor NM3 is OFF. Now this right side of bootstrapped capacitor C0 will get connected to gate of transistor PM0 because transistor NM2 is ON. Due the voltage change that occur at the left side of bootstrapped capacitor C0 from 1v to 0.001v, Va changing from 1v to 0.001v then right side of bootstrapped capacitor C0 will change from 0v to -0.506v i.e. node V2p changes from 0v to -0.506v means internal voltage undershoots. The extend of internal voltage undershoots is calculated by the ratio of bootstrapped capacitor C0 to the parasitic capacitance at the right side of C0. Due to this voltage undershoots the output voltage can switch at faster rate since gate voltage of transistor PM0 is driven at -0.506v. As shown in figure 2 output voltage can go up to full swing of 1.00001v. The pull down transient operation has complementary working as pull up transient. In this conventional bootstrapped driver circuit value of bootstrapped capacitors are C0 = 350fF, C1 = 250fF. Sizing of all PMOS transistors width/length = 800nm/180nm, all NMOS transistors width/length = 400nm/180nm.

## 4. PROPOSED BOOTSTRAPPED DRIVER AT 180NM TECHNOLOGY

This modified bootstrapped driver circuit when used at 180nm technology of cadence virtuoso the minimum input supply voltage which we can give to this circuit is 0.8v or 800mv. In this modified bootstrapped driver circuit input supplied is pulse with period of 20ns and pulse width of 10ns. Here two bootstrapped capacitors are used i.e. Cp=Cn=17 femto farad. Using this output voltage boost to 1.2 volt. In the circuit diagram of modified bootstrapped driver Cp and Cn are bootstrapped capacitor PM1 and NM2 are transistor for Cp precharge and Cn predischarge. V2p and V2n are the boosted nodes. Output from transistors PM3 and NM3 will act as inverter output and this output Va is used to control PM2 and NM1. Final vout is the output voltage of modified bootstrapped driver that is boosted above Vdd and below GND. Using this driver output we can drive further circuitry that work on low voltages. When Vin is transiting from high to low, initially node V2n is at 0v. After transiting from high to low i.e. when Vin= 0v, then node V2n will be boosted to -587.718mv. At this moment transistor PM2 turned OFF and NM1 turned ON. Therefore boosted signal at node V2n pass from NM1 and reach at Vout.

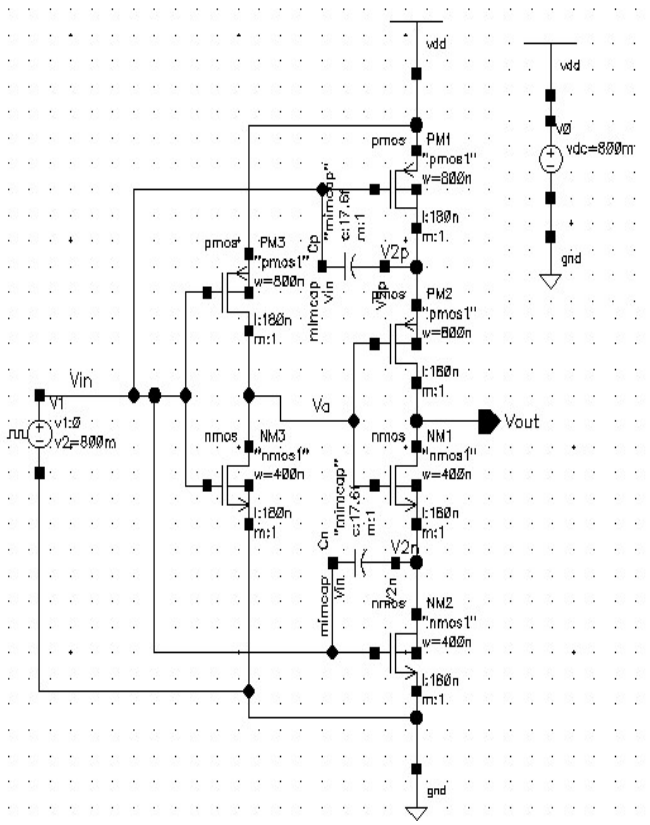


**Fig-3:** Proposed bootstrapped driver circuit at 180nm

At the same time when Vin=0v, the transistor PM1 is ON to precharge node V2p to VDD is 0.8v or 800mv. However NM2 is turned ON reversely causing the reverse current flow to charge V2n, when Vin is low or 0v. At the end of period node V2n still holds the charge -250.193mv. Now when Vin is HIGH, transistor PM1 gets OFF, Node V2p is boosted above VDD i.e. upto 1.4v. At the end of period it still holds charge 1.197v. At the same time as vin is 0.8v, then PM2 turned ON and NM1 turned OFF. So node V2p is boosted upto 1.475v and this will go to Vout through transistor PM2 At the same moment NM2 is turned ON it will precharge capacitor Cn to -12.9994uv or below GND. So final output voltage which we get after complete swing of Vin, when it transit from LOW to HIGH and HIGH to LOW is when Vin is 0.8v then output voltage Vout will boost above Vdd to 1.3v. When Vin is 0v then output voltage will boost below Gnd to -366.843v. Figure 4 shows the simulated waveform of proposed bootstrapped driver circuit at 180nm technology.

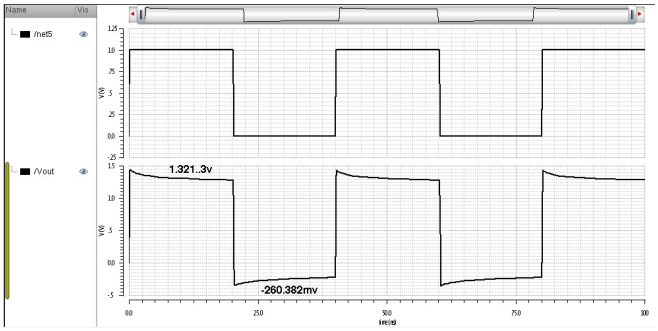


**Fig-4:** Output waveform of proposed bootstrapped driver

## 5. LAYOUT OF PROPOSED BOOTSTRAPPED DRIVER

I have made layout of modified bootstrapped driver at CADENCE Virtuoso 180nm technology using bootstrapped capacitors of 17 femto farad. These two bootstrapped capacitors are mimcap having width of 4um and length of 4um. This is the minimum size capacitor which I have used in my modified design. If we increase these capacitor value then our capacitor sizes also get increased which make layout are to get increased. According to this modified bootstrapped driver layout, layout area covered is

Layout area= 13.345um*12.745um

= $170.082025*10^{-12}$ $m^2$ or 0.170 $nm^2$

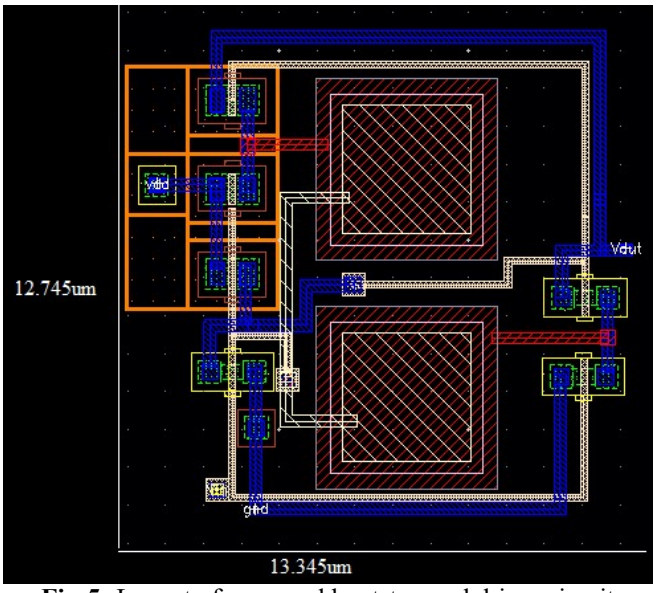


**Fig-5:** Layout of proposed bootstrapped driver circuit

## 6. POST LAYOUT SIMULATION OF PROPOSED BOOTSTRAPPED DRIVER CIRCUIT

Figure 6 below shows the configuration circuit of proposed bootstrapped driver circuit in which Vin = 1v is supplied.

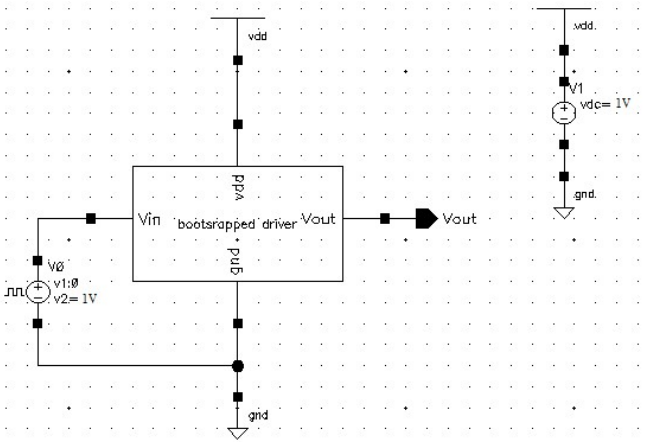


**Fig-6:** Configuration circuit of proposed bootstrapped driver circuit

Figure 7 below shows the post layout simulation response of proposed bootstrapped driver circuit at 180nm technology.

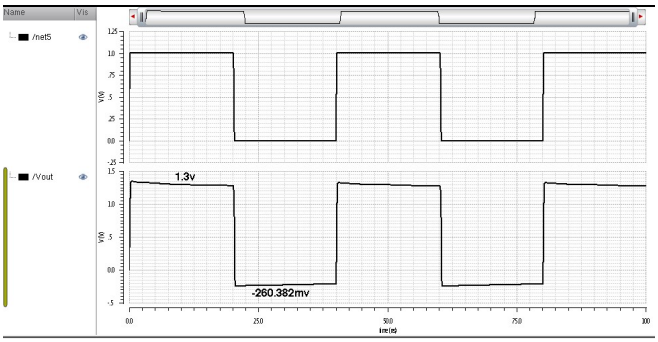


**Fig-7:** Output response of post layout simulation of proposed bootstrapped driver

## 7. RESULTS AND DISCUSSION

In figure 8 below shows the comparison of output voltages in bootstrapped driver circuits designed at CADENCE virtuoso 180 nm and 90 nm technologies. From this figure it is clear that proposed bootstrapped driver circuit gives better results as compared to conventional bootstrapped driver circuit.

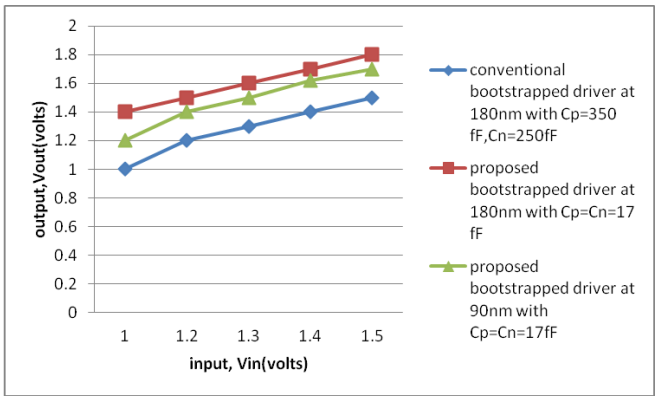


**Fig-8:** Comparison of vin and vout of bootstrapped driver circuits

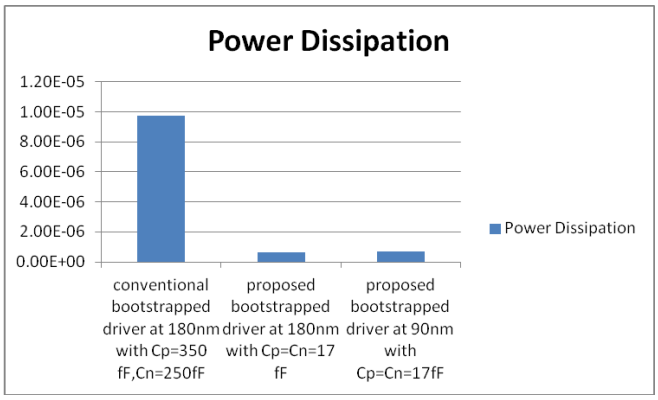


**Fig-9:** Comparison of power dissipation of bootstrapped driver circuits

Figure 9 shows the comparison of power dissipation occurs in different bootstrapped driver circuits. In conventional bootstrapped driver circuit power dissipation is 9.73E-06, in

proposed bootstrapped driver at 180nm power dissipation calculated is 6.57E-07 and in proposed bootstrapped driver at 90nm PD = 6.83E-07

Figure 10 shows the comparison of delay occurs in different bootstrapped driver circuits. In conventional bootstrapped driver circuit delay = 20.08E-9, in proposed bootstrapped driver circuit at 180nm delay = 20.07E-9 and in proposed bootstrapped driver circuit at 90nm delay = 20.03E-9.

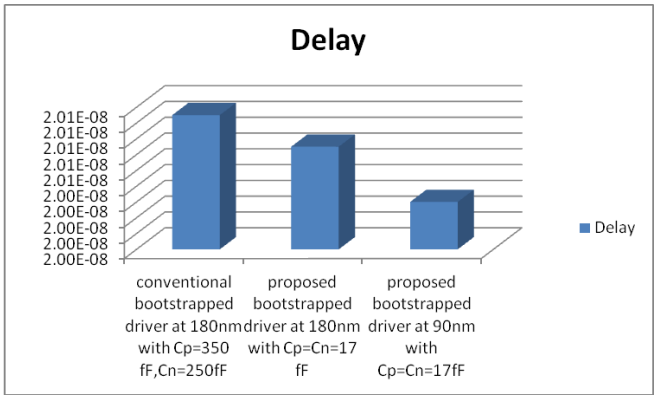


**Fig-10:** Comparison of delay occur in bootstrapped driver circuits

Figure 11 shown below compares the leakage current occurs in different bootstrapped driver circuits. In conventional bootstrapped driver circuit leakage current = 3.50E-12, in proposed bootstrapped driver circuit at 180nm leakage current = 3.49E-12 and in proposed bootstrapped driver circuit at 90nm leakage current = 9.78E-11.

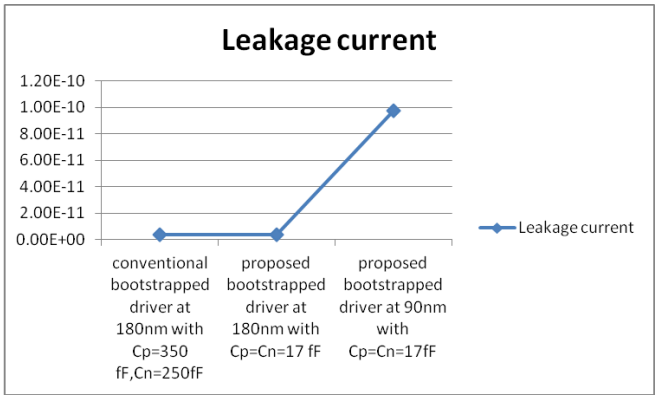


**Fig-11:** Comparison of leakage current occur in bootstrapped driver circuits

**Table-1:** Transistors sizing in bootstrapped driver

| PARAMETER | PMOS W/L | NMOS W/L | Total number of transistor PMOS/NMOS |
|---|---|---|---|
| Conventional bootstrapped driver at 180nm with Cp=350 fF,Cn=250fF | 800nm/180nm | 400nm/180nm | 5/5 |
| Proposed bootstrapped driver at 180nm with Cp=Cn=17 fF | 800nm/180nm | 400nm/180nm | 3/3 |
| Proposed bootstrapped driver at 90nm with Cp=Cn=17fF | 360nm/150nm | 120nm/150nm | 3/3 |

## 8. CONCLUSION

In this paper I have explained about bootstrapped technique and shown how we can use that technique in driver circuits. The proposed driver circuit gives better results compared to conventional driver circuit with low power dissipation less delay and less leakage current. Proposed bootstrapped driver circuits are designed at CADENCE virtuoso 180nm as well as 90nm technology. From layout of proposed bootstrapped driver circuit it is verify that proposed driver circuit occupy less area. In GDI technology which cascaded transistor (PTL) there is a serious problem of degradation of output level after some stage, level restoration logic is required to achieve the output voltage level. Above bootstrap circuit can also be used for logic restoration devices to maintain the constant voltage for logic.

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## BIOGRAPHIE

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