DESIGN AND IMPLEMENTATION OF 15-4 COMPRESSOR USING 1-BIT SEMI DOMINO FULL ADDER AT 28nm TECHNOLOGY

G.Raju¹, S.Aruna², G.Ranjith Kumar³, S.Vasu Krishna⁴

¹Student, ECE Dept., MVSR Engineering College, Hyderabad, India ²Asst. Prof., ECE Dept., MVSR Engineering College, Hyderabad, India ³Staff Design Engineer at SM Silicon India Pvt. Ltd., Hyderabad, India ⁴Associate Prof., ECE Dept., at Geethaniali College of Engg. & Tech., Hyderabad, India

Abstract

In this paper, we present 15-4 Compressor for Digital signal processing. A new Low power full adder and 5-3 compressor are used in this 15-4 compressor. Full Adder and 5:3 compressors are realized by Semi Domino logic which is faster and consumes less power than other conventional logics. Objective of this Work is to inspect the power, delay, power delay product of full adders in different logic styles and to inspect power, delay, and power delay product of Semi domino 5-3 compressor architecture with other architectures. Simulation results demonstrate the superiority of the proposed adder circuit against the pre-proposed adder circuits in terms of power, delay, PDP. The proposed style gets its benefit in terms of power, delay, PDP. The performance of the adder circuits and compressors is based on TSMC 28nm CMOS process models at the supply voltage of IV, 500MHz frequency evaluated by the comparing of the simulation results obtained from Cadence spectre.

***______

Keywords: Semi Domino Logic, Full adder, 5-3 compressor, power, delay, PDP, TSMC 28nm.

1. INTRODUCTION

DIGITAL signal processing area is widely used in order to perform complex operations like DFT (Discrete Fourier transform), FFT (Fast Fourier transform), convolution, filtering [12] and etc. Multiplier is the basic block required for many signal processing applications. Full adder is the foundation element of complex arithmetic circuits like addition, multiplication, division, exponent circuits

A 1-bit full adder adds binary numbers and accounts for values carried in sum out. A single-bit full adder adds three single-bit numbers, often written as A, B, and Cin. The A and B used as operands and Cin bit are carried in from the succeeding least significant stage. Adder circuits produce Double-bit output, carry-out and sum typically represented by the signals Cout and Sum, Thus, enhancement of the performance of the adder block directs to the improvement of the overall system performance [11].

Multiplication is the complex operation which consumes most of the processing time and power. So designing the high speed multiplier is one of the challenging tasks. The multiplication process mainly consists of three steps 1. Partial product generation 2.Partial product reductions 3.Final carry propagating addition. Reduction of partial product takes much time and power in the multiplier. Many techniques have been proposed to reduce vertical critical path in the multiplier. Using compressor in partial products reduction step is so popular. Compressors are basic circuits which counts the number of ones in the given input. There are many compressors available e.g. 3-2 compressor, 4-2 compressor, 5-2 compressor and 7:2 compressors.

Digital signal processing involves large multiplication (to perform complex operation) where multiplier and multiplicand exceeds 128bit or more. For such operations, using of small compressors like 5-2 and 7-2 would not give better performance in terms of speed and power. Design of higher bit compressor is required for such applications. This paper is focused on 15-4 compressor which can be used for multiplier. This multiplier can be used in many signal processing applications.

This paper is structured as: Section II realizes the basic adder designs using conventional logic styles. The Semi Domino full adder is analyzed in section III. Section IV realizes the 5-3 compressor architectures. Section V of the paper is implementation 5-3 compressor and full adder in 15-4 compressor. Section VI is conclusion of the paper. Section VII is acknowledgement of the work.

2. PREVIOUS WORK ON FULL ADDERS

The selection of a logic design style is inclined to a number of factors namely layout area, speed of circuit and power dissipation, noise tolerance, process technology, and used supply voltage etc. While dynamic circuits can be used to implement high-speed logic gates, there are anxieties over Leakage currents and high power dissipation. Hence, the focus will be on static CMOS logic families in this paper. The following three full adders that are representative of various CMOS logic design styles will be considered.

The conventional static CMOS full adder [13] cell is shown in figure 1. It contains 28 transistors and is based on NPCMOS logic style. Any gate in this design method consists of complementary logic networks composed of PMOS for pull-up and NMOS devices for pull-down. The design guarantees the output node moves to and fro between the positive rail and ground so that the static power dissipation of the circuit is negligible. PMOS devices will be 'ON', if input is 'logic0' and NMOS devices will be 'ON', if input is 'logic1'.

Static CMOS logic is a traditional logic family known for ease of design, a good noise margins, low power dissipation, and robustness of the circuit. A 28 transistors mirror adder design, was selected as the representative static CMOS design. The schematic is shown in Figure.1.





Fig 2: Conventional dynamic logic (CDL) full adder

The conventional dynamic logic (CDL) full adder [11] cell is shown in Figure 2. It is having 16 transistors and is based on NP-CMOS logic style. The dynamic adder although having higher speed and Small in size but consumes more amount of power.

The complementary pass-transistor logic (CPL) full adder [5] is shown in Figure 3. It has 32 transistors and is based on the CPL Logic. It provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of the cross coupled PMOS transistors. But owing to the presence of a lot of internal nodes and static inverters, there is huge power dissipation.



3. SEMI-DOMINO FULL ADDER

3.1 Circuit Analysis

A new adder cell is presented in this paper Figure 4. This Circuit consists of two precharge transistors (M1, M8), evaluation networks to evaluate carry and sum (PDN Carry, PDN Sum), two keeper transistors (M2, M9), six footer Transistors (M3, M4, M5, M10, M11, M12) and two semidomino inverters. Through the precharge phase when the CLK is LOW, the pre-charge PMOS transistor becomes ON and the dynamic node is connected to the VDD and obtains precharge from VDD. When clock goes high, the evaluation phase starts and the output gets evaluated with the pulldown network and conditionally gets discharged if any one of the inputs stays at logic 1.

At the evaluation stage when all the inputs are at logic 0, the dynamic node becomes logic 1. But more fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the subthreshold leakage. This charge is compensated by the PMOS keeper, which we want to recapitulate the voltage of the dynamic node. At a time when, noise voltage impulse comes at gate input, the keeper may not be able to restore the voltage level of the dynamic node. To stop that the footers M3, M4 and M5 and the M10, M11 and M12 are connected to the carry and sum part. M3 and M10 operate as stack transistors. At the evaluation phase when PDN of sum and carry are at logic 1, at that time M3 and M10 stops the free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node of carry and sum simultaneously. To compensate that M5 and M12 make a charge discharge path for the carry part and the sum part simultaneously.



Fig 4: Semi Domino Full adder

The output node pulse N_Dyn always propagated by turning 'ON' the NMOS transistor of the buffer by the precharge pulse in dynamic node. We have connected the source of the buffer's NMOS transistor M7 and M14 to the drain of the NMOS clock transistor (N_FOOT) instead of GND, which Operates in semi-domino logic. In this ongoing section we will go through some mathematical analysis for noise and power saving which can demonstrate the enhancements and Advantages of the circuit.

In the evaluation period of the carry part, when the NMOS Clock transistor M3 is ON, at that time N_Foot node gets discharged to 0. When the pull down network gets ON the N_Dyn will discharge to ground. This leads to the VGS of buffer NMOS M7 to 0 as VGS=VG-VS=0. In this situation, the NMOS is OFF and the buffer output gets completely charged through PMOS M7.

During precharge period, the dynamic node gets precharged to HIGH, when the PDN is ON the voltage of the N_Foot is nearly same as N_Dyn, as the NMOS M3 is OFF. The VGS of the buffer NMOS will be at VG - VS < VTH. This VTH voltage turns the NMOS of the buffer OFF. The PMOS of the buffer is also OFF due to the high level of N_Dyn node. This condition makes the output of buffer LOW.

3.2 Results and Discussions

In the Semi Domino circuit, the precharge pulses are prohibited to pass to the output node of buffer stage. This results in decreasing the power consumption in the output stage. Ideally the precharge pulses propagate completely to the output. In this circuit this propagation is prohibited.



Table1: Comparison of Full Adders

Adder	Delay	Power	PDP			
CMOS	1.46E-11	2.05E-06	2.99E-17			
CPL	1.30E-11	27.8E-06	36.1E-17			
Dynamic	1.2E-11	36.4E-06	43.6E-17			
Semi	1.1E-11	1.51E-06	1.66E-17			
Domino						

Table 1 gives the analysis of different adders in terms of power, delay and power delay product. Semi Domino full adder PDP is better when compared to other Full adders. So we can use it for low power applications

3.3 Layouts of Full Adders

Layout is the drawing of masks used in the manufacturing process. The layout we draw is not perfectly reproduced on the wafer. We must comply with a set of rules to ensure that the layout we draw is manufactural.



Fig 6 (a): CMOS full adder layout



Fig 6 (b): CPL full adder layout



Fig 6(c): Semi domino full adder layout



Fig 6(d): Dynamic Full adder layout

Figure 6(a), 6(b), 6(c), 6(d) are layouts of full adders. Cadence layout editor is used for layouts. We followed 28nm DRC and LVS rules for all layouts.

4. 5-3 COMPRESSOR

A combinational logic circuit of 5-3 compressor is a topology accepting five inputs and generating three outputs. The five input bits are summed up to produce the three bit output. The conventional design of 5-3 compressor is an enhanced version of 4-2 compressor and can have maximum value of 101 when all the inputs are 1. The conventional Architecture of 5-3 compressors is shown in Figure 7.

In multipliers partial product reduction is most important thing. So, if we use higher order compressor we can reduce the delay and power during partial product reduction stage. 5-3 compressor is generally consist of 2 full adders and 1 half adder.



Fig 7: 5-3 compressor

Sum of first full adder (s0) is given to the next full adder, Last stage of 5-3 compressor is half adder, and it takes the carry outputs from both full adders. Carry of the half adder is MSB of the 5-3 compressor and second full adder sum is LSB of it. Full adders and half adders are made of Semi domino logic, so its power dissipation will be less .Every block will evaluate based on clock. In precharge mode all blocks will precharge to VDD i.e., 1 v and during evaluation mode it counts the number of 1's given to it.Truth table of the 5-3 compressor is given in table 2

Table2: Truth table of 5-3 Compressor

		1	
Inputs	03	O2	01
All the inputs are 0	0	0	0
Any one input is 1	0	0	1
Any two inputs are 1	0	1	0
Any three inputs are 1	0	1	1
Any Four inputs are 1	1	0	0
All inputs are 1	1	0	1

Table2 describes the working of 5-3 compressor. It ignores 0's and adds number of 1's given to it and produces corresponding output. If all inputs are logic 1, then it generates 101. This is the maximum logic which is accepted by 5-3 compressor.



Fig 8: Simulation results of 5-3 compressor

Compressor	Delay	Power	PDP
CMOS	6.3e-12	11.45e-06	7.21e-17
CPL	15.1e-12	35.6e-06	53.7.e-17
Dynamic	7.12e-12	90e-06	64.08e-17
SemiDomino	6.2e-12	5.9e-06	3.65e-17

Compared to other Compressor architectures Semi domino 5:3 compressor architecture consumes less power and it provides high speed. So we use this 5-3 in higher order compressors like 15-4 compressor for fast reduction of partial products and to reduce power of processor.

5. DESIGN OF 15-4 COMPRESSOR

The basic architecture of 15-4 compressor [2] is shown in Figure 9.This will compress 15 partial products into four outputs. It has five full adders and two 5-3 compressors and one parallel adder. Each full adder is used to compress three partial products into sum and carry.

All the sums from five full adders are compressed with the help of proposed 5-3 compressor and carry outputs are compressed with the help of proposed 5-3 compressor. Parallel adder is used to add the output of 5-3 compressors. Inputs of 4 bit parallel adder (B3 and A0) are grounded.

Semi domino Full adder and 5-3 compressors are implemented in first and second stage of 15-4 compressor respectively. Last stage in the 15-4 compressor is parallel adder. It is shown in Figure 10. Here have 2 half adders and 1 full adder to realize parallel adder. Two inputs of parallel adder are grounded (i.e., A0, B3).S0 doesn't depend on other logic, so it is directly coming same as B0. Because each state can be achieved from the earlier stage, the decision value is represented by one bit. If the bit is '1' the path selected is coming from the lower state from those two possible states in the trellis diagram, and if the decision bit is '0' the path selected is coming from the upper state



5.1 Results

Waveforms of 15-4 compressor is shown in Figure 11s.we have 15 inputs and 4 outputs. Outputs will be generated when clock is high i.e., evaluation mode.



6. CONCLUSION

In this paper, we have designed and analyzed a full adder cell based on semi domino logic at TSMC 28 nm process technology using cadence specter .We have realized the circuit and compared conventional adder circuits with Semi Domino full adder. The simulation results shows that this semi domino adder has better performance than the previous proposed conventional circuits. The architecture of 5-3 compressor is analyzed using Semi domino full adder. This adder and 5-3 compressor are used in 15-4 compressor. Semi domino compressors (5-3 and 15-4) design gives better result than conventional compressors. This 15-4 compressor can be used to design the large multiplier.

ACKNOWLEDGEMENTS

The proposed work was carried out in Startup Company working on ASIC based designs in Hyderabad. This work was greatly supported by MVSR Engineering College, Hyderabad.

REFERENCES

[1]. Meher, P.; Mahapatra, K.K., "Low power noise tolerant domino 1-bit full adder," *Advances in Energy Conversion Technologies (ICAECT), 2014 International Conference on*, vol., no., pp.125,129, 23-25 Jan. 2014

[2]. Marimuthu, R.; PradeepKumar, M.; Bansal, D.; Balamurugan, S.; Mallick, P.S., "Design of high speed and low power 15-4 compressor," *Communications and Signal Processing (ICCSP), 2013 International Conference on*, vol., no., pp.533,536, 3-5 April 2013

[3]. Ohsang Kwon,Kevin Nowka, Earl E. Swartzlander, Jr," A 16-Bit by 16-Bit MAC Design Using Fast 5:3 Compressor Cells", Journal of VLSI Signal Processing 31, 77–89, 2002
[4]. J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits- A Design Perspective", 2nd Prentice Hall, Englewood Cliffs, NJ, 2002 [5]. R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass transistor logic", IEEE Journal of Solid-State Circuits, Vol. 32, pp. 1079–1090, July 1997.

[6]. H.L. Yeager et al, "Domino Circuit Topology", U. S. Patent 6784695, Aug. 31, 2004.

[7]. F. Mendoza-Hernandez, M. Linares-Aranda and V. Champac, "Noise tolerant improvement in dynamic CMOS logic circuit", IEEE Proc.-Circuits Devices Systems, Vol 153, No. 6, Dec 2006, pp. 565-573

[8]. Meher, P.; Mahapatra, K.K., "A high speed low noise CMOS dynamic full adder cell," *Circuits, Controls and Communications (CCUBE), 2013 International conference on*, vol., no., pp.1,4, 27-28 Dec. 2013

[9]. Mahmoodi-Meimand, H.; Roy, K., "Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.51, no.3, pp.495,503, March 2004

[10]. Chowdhury, S.R.; Banerjee, A.; Roy, A.; Hiranmay Saha, H., "Design, Simulation and Testing of a High Speed Low Power 15-4 Compressor for High Speed Multiplication Applications," *Emerging Trends in Engineering and Technology, 2008. ICETET '08. First International Conference on*, vol., no., pp.434,438, 16-18 July 2008

[11]. J. Uyemura, "CMOS Logic Circuit Design", ISBN 0-7923-8452-0, Kluwer, 1999.

[12]. Mateus Beck Fonseca, Jo[°]ao Baptista S. Martins, Eduardo A. C[°]esar da Costa," Design of power efficient butterflies from Radix-2 DIT FFT using adder compressors with a new XOR gate topology", Analog Integr Circ Sig Process (2012) 73:945–954.

[13]. N.Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective," Addison Wesley, 1993