SYNCHRONOUS FLYBACK CONVERTER WITH SYNCHRONOUS BUCK POST REGULATOR

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Abstract

In general, conventional converter is used for converting the power level from one stage to another. But conventional type of converter has slightly more power losses & voltage drop, so efficiency is very sensitive for the low voltage specification and also cooling of dissipative elements floating at higher voltages is a difficult task. So high efficient scheme of synchronous flyback converter with synchronous buck post regulator was approached and low voltage drop, less power losses & very high efficiency was achieved. Where the secondary side of flyback converter including Synchronous buck post regulator floats on the very high voltage line (i.e. 10kV) for the Filament power supply heats the cathode to required temperature to emit electrons in TWT. Filament Power supply based on the Fly back Converter topology which is operated at 100 KHz in CCM mode The Pulse width modulation technique is used to maintain the voltage at desired value using IC. The Post regulator using Synchronous buck topology is implemented for regulating the output voltage of synchronous flyback converter (9.5V DC) to Regulated 6.3V @ 3.3A DC.

Keywords: *CCM (Continuous current mode), Pulse width modulation (PWM), synchronous Buck Regulator, Synchronous Flyback converter, TWT (Travelling Wave Tube), SR (Synchronous Rectifier).*

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1. INTRODUCTION

The conduction loss of diode rectifier contributes significantly to the overall power loss in a power supply, especially in low output voltage applications. The rectifier conduction loss is proportional to the product of its forward-voltage drop, V_F, and the forward conduction current, I_F [1].

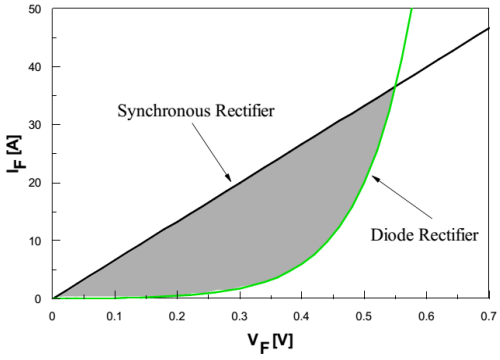


Fig -1: Forward-voltage comparison between synchronous rectifier and diode rectifier. ▭ area has conduction loss saving by using synchronous rectifiers [1].

On the other hand, operating in the MOSFET III quadrant, a synchronous rectifier presents a resistive i-v characteristics, as shown in Fig.1.

Under certain current level, the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier, and consequently reduces the rectifier conduction loss. Due to the fact that synchronous rectifiers are active devices, the design and utilization of synchronous rectification need to be properly addressed.

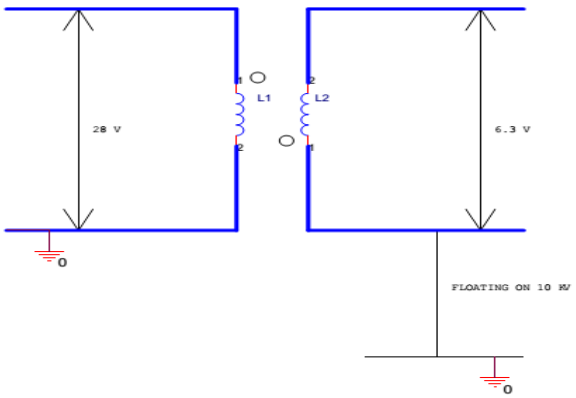


Fig -1.1: Flyback Transformer

This paper analyses the application of synchronous rectification in two most popular topologies, flyback & Buck converters. The limits of efficiency improvements that can be

obtained using synchronous rectification are determined. Conversion efficiencies of different implementations are compared, and verified with experimental evaluations. Here secondary side of flyback converter will be floating on very high voltage line (i.e. 10kV or more). So it is very difficult to take feedback signal for control circuit from secondary side of synchronous flyback converter to primary side, because voltage level of primary side is 28V DC whereas voltage level of secondary side of flyback converter is 10kV with respect to ground, as shown in fig. 1.1. Hence there is a need for highly efficient post regulator as a next stage to the flyback converter to obtain regulated 6.3V DC from 28±0.5V DC input. Highly efficient post regulator was implemented using synchronous buck topology.

2. SYNCHRONOUS FLYBACK CONVERTER

A flyback converter with the SR (Synchronous Rectifier) is shown in Fig 2. For proper operation of the converter, conduction periods of primary switch SW and secondary-side switch SR must not overlap.

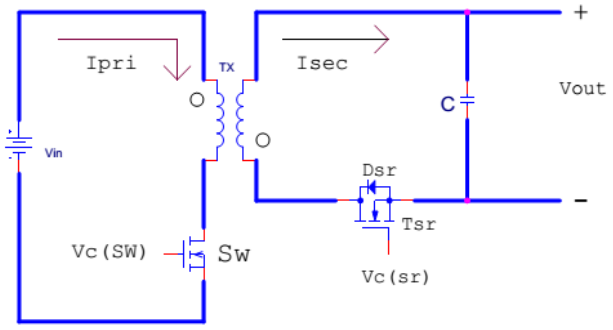


Fig -2: Synchronous flyback converter

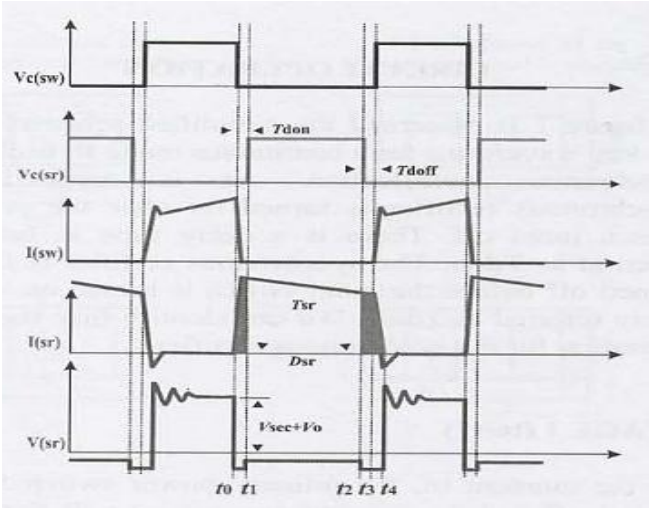


Fig -2.1: Expected waveform of synchronous flyback converter [2].

To avoid the simultaneous conduction of the SW and the SR, a delay between the turn off instant of switch SW and the turn-on instant of the SR as well as between the turn-on instant of the SW and turn-off instant of the SR must be introduced in the gate-drive waveforms of the switches as in Fig 2.1[2]. With properly designed gate drives, the operation of the circuit shown in Fig.2 is identical to that with a conventional diode rectifier. Namely, during the time switch SW is turned on, energy is stored in the transformer magnetizing inductance and transferred to the output after SW is turned off.

2.1 Design and Simulation Result of SR Flyback Converter:

Specifications:
Input Voltage V_{in} (dc) = (28±0.5) V,
Switching Frequency = 100 KHz,
Outputs Specifications: (9.5V, 2A), $P_{0\,min}$ = 6 watts

Step 1: Establish primary & secondary turn Ratio:

$$\frac{N_p}{N_s} = \frac{(V_{dcmin} - 1)D_{max}}{(1 - D_{max})(V_0 + 1)} = 2.0649 \quad (1)$$

Where D_{max} = 0.45 (assumed)

Step 2: Voltage stress of main switch (SW):

$$V_{ms\,max} = V_{dc\,max} + \frac{N_p}{N_s} * (V_0 + 1) = 50.182\ V \quad (2)$$

Where $V_{dc\,max}$ = Maximum dc input voltage.
$V_{ms\,max}$ = Maximum stress on the device (2*$V_{dc\,max}$).
N_P = Primary no of turns.
N_s = Secondary no of turns (main output).
V_0 = Output Voltage.

Step 3: Calculation of primary magnetizing Inductance (Lp):

$$L_p = \frac{(V_{dc\,min} - 1) * V_{dcmin} * (T_{onmax})^2}{2.5 * P_{0min} * T_S} = 98.38\mu H \quad (3)$$

Where, given: f = 100 kHz, D= 0.45, $P_{0\,min}$= 6 watts; S0, T=1/f = 10 µs; $T_{on\,max}$ = D* T = 4.5 µs. (4)

Step 4: Calculation of primary peak current (I_{cpr}):

$$I_{cpr} = \frac{1.25 * P_{0max}}{V_{dcmin} * D_{max}} \quad (5)$$

(Assuming 80% efficiency)

= 1.919A

Ramp amplitude dI_p

$$dI_p = \frac{2.5 * P_{o\,min}}{V_{dc\,min} * D_{max}} \quad \text{(Let } P_{0\,min} = 6W\text{)} \quad (6)$$

= 1.21A

Therefore peak current in the mosfet = Icpr + (dIp/2) (7)

= 2.52A

Step 5: Calculation of secondary peak current (I_{csr}):

$$I_{csr} = \frac{P_{o\,max}}{V_o(1-D_{max})} \quad (8)$$

= 3.6A

Average of I_{csr} gives secondary load current

i.e., $I_{csr}\,(1-D_{max}) = 1.98A$ (9)

Step 6: Output filter capacitor C_0:

$$C_0 = \frac{D_{max} * P_0}{F_{sw} * V_0 * \Delta V_0} \quad \text{(Take } \Delta V_0 = 39mV\text{)} \quad (10)$$

= 231µF

Choose a cap of C_0=300µF.

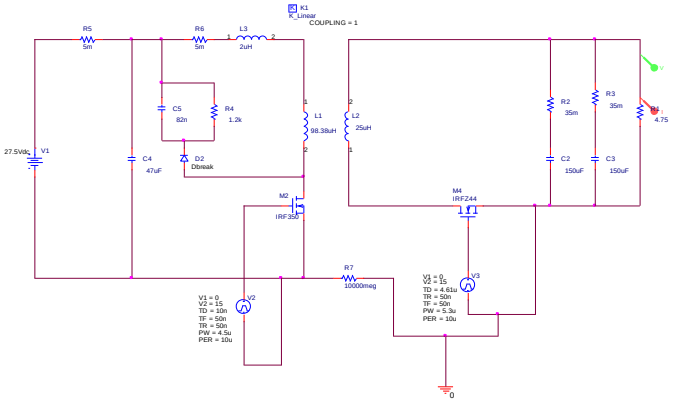


Fig -2.2: Simulation circuit of SR flyback converter

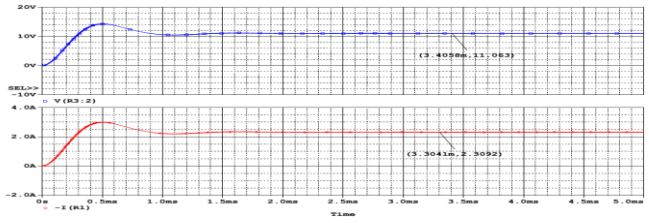


Fig -2.3: Output voltage and current of synchronous flyback Converter

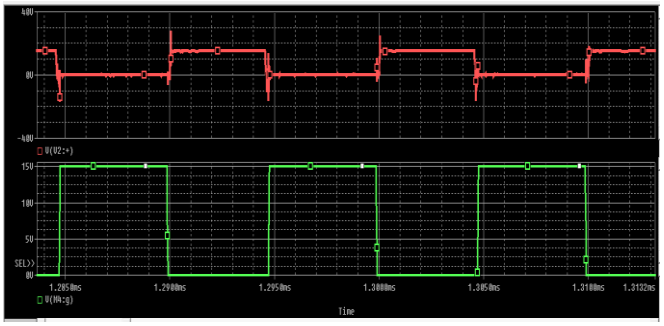


Fig -2.4: Gate pulse of primary and secondary mosfet

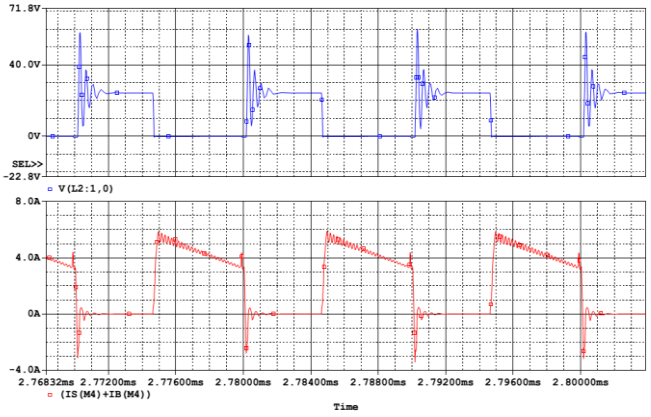


Fig -2.5: Waveform of V(sr) and I(sr) of mosfet (M4).

2.2 Transformer Design

Area product of flyback converter:

$$A_p = \left[\frac{L_p * I_{peak} * I_{rms} * 10^4}{420 * k * B_{max}}\right]^{1.31} \quad (11)$$

Where A_p = area product in cm^4, K= winding factor, 0.2 for continuous mode flyback, $B_{max} = B_{sat}$ in tesla @ 100°C

$$I_{rms} = \sqrt{D_{max} * \left[(I_{peak})^2 - \Delta I_L * I_{peak} + \frac{(\Delta I_L)^2}{3}\right]} \quad (12)$$

=1.3058A, where $\Delta p = \Delta I_L$ =1.21A

Therefore area product required

$$A_p = \left[\frac{L_p * I_{peak} * I_{rms} * 10^4}{420 * k * B_{max}}\right]^{1.31} \quad (13)$$

=0.29 cm^4 = 2900 mm^4

Now select ETD 39 Core and core material is N87.

A_e = 125 mm^2 for N87

Calculation of primary turns

$N_p = (L_p * I_p)/ (B_m * A_e)$ (14)

N_p = 8 turns, so taking N_p = 10 turns

Calculation of secondary turns N_s

$\frac{N_p}{N_s}$ = 2.065

Ns = 5 Turns.

Primary and secondary wire selection:

Skin depth calculation

Skin depth = $\frac{66}{\sqrt{f_s}}$ mm (15)

f_s = switching frequency =100 kHz

Skin depth= $\frac{66}{\sqrt{100K}}$

=0.2087mm

So, wire diameter should be < 2* 0.2087mm.

Now wire selection is done accordingly and 10kV isolation requirements between primary/secondary windings and secondary winding/core are met using polyimide sheet in flyback Transformer, as shown in Fig. 2.6.

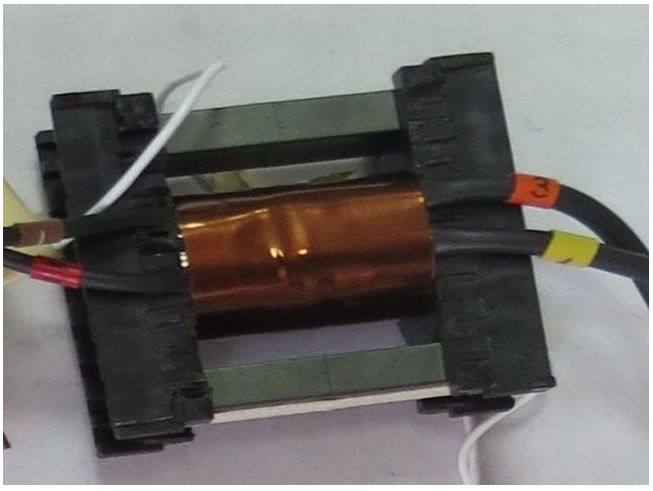


Fig -2.6: ETD core Transformer.

2.3 PWM Controller for Synchronous Flyback Converter

UC28025: For primary side control of SR flyback converter PWM IC UC28025 is used, which is a fixed-frequency PWM controller optimized for high-frequency SMPS applications. Targeted for cost effective solutions with minimal external components, UC28025 include an oscillator, a temperature compensated reference, a wide band width error amplifier, a high-speed current-sense comparator and high-current active-high totem-pole outputs to directly drive external MOSFETs.

FAN6204: FAN6204 is selected for secondary side of synchronous rectification (SR) controller. FAN6204, which is suitable for Continuous Conduction Mode (CCM) and also suitable for Discontinuous Conduction Mode (DCM) / Quasi-Resonant (QR) flyback converters and dual-switch forward free-wheeling rectification (Figure 2.7) [7]

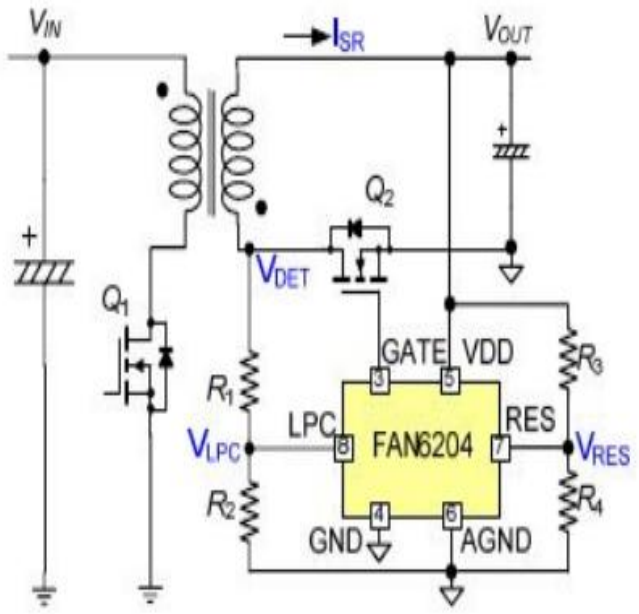


Fig -2.7: Typical Application Circuit for Flyback Converter[7].

FAN6204 utilizes a proprietary innovative linear-predict timing control to determine the turn-on and turn-off timing of SR MOSFET [7]. This control technique detects the voltage of the transformer winding and output voltage instead of MOSFET current, so noise immunity can be accomplished. Furthermore, this technique doesn't need a communication signal from the primary side, so this feature reduces external components and simplifies PCB layout. This is also easier for implementation, in high voltage applications, where transferring timing signals across the isolation barrier is difficult.

3. SYNCHRONOUS BUCK REGULATOR

The simplest way to get a regulated output by using linear regulator, but with linear regulators there is a dissipation of the order of 1.5 to 2W for any 15 to 20W converters which makes heat removal from the elements floating at higher voltages cumbersome. Hence there is a need for switching post regulator. Buck converter (step down) is the simplest solution but Synchronous Buck regulator, on the other hand, can be remarkably efficient (95% or higher).

3.1 Asynchronous Buck Topology

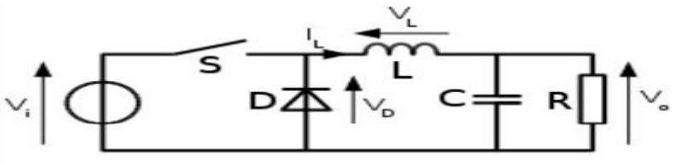
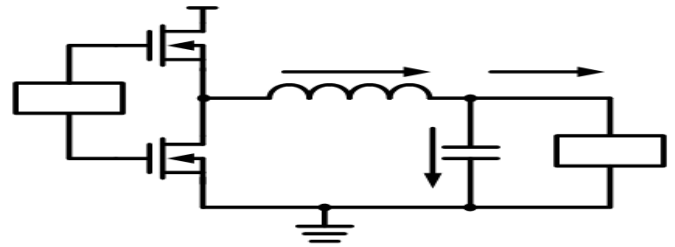


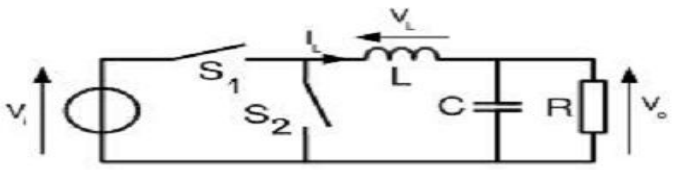
Fig -3.1: Asynchronous buck converter

A typical asynchronous buck regulator circuit is as shown in the figure 3.1 above. 'S' denotes a MOSFET being used in the top side with a diode 'D' in the bottom side. These are the two main switches that control power to the load. When the MOSFET is turned ON, V_{IN} charges the inductor 'L', capacitor 'C' and supplies the load current. Upon reaching its set output voltage the control circuitry turns OFF the MOSFET (hence called a switching MOSFET). Switching OFF the top side MOSFET disrupts the current flowing through the inductor. With no path for the current, the inductor will resist this change in the form of a catastrophic voltage spike. To avoid this spike when the top side MOSFET is turned OFF, a path is provided for the inductor current to continue flowing in the same direction as it did before. This is created by the bottom side diode 'D'. When the top side MOSFET turns OFF, the inductor voltage reverses its polarity forward biasing the diode 'D' on, allowing the current to continue flowing through it in the same direction. When current flows in the diode, it is also known as being in freewheel mode. When the output voltage drops below the set point, the control will turn ON the top side MOSFET and this cycle repeats to regulate the output voltage to its set value.

3.2 Synchronous Buck Topology



(a)



(b)

Fig -3.2: (a) and (b) Simplified schematic of a synchronous converter, in which D is replaced by a second switch,S2.

The synchronous topology is depicted in the fig.3.2 above. The bottom side diode 'D' has been replaced with another MOSFET, 'S2.' Since there are two MOSFETs 'S1' is called the high-side MOSFET and 'S2' the low-side MOSFET. The low-side MOSFET is also referred to as the synchronous MOSFET while the high-side MOSFET is called the switching/control MOSFET. In steady state, the low-side MOSFET is driven such that it is complimentary with respect to the high-side MOSFET. This means whenever one of these switchesis ON, the other is OFF. In steady state conditions, this cycle of turning the high-side and low-side MOSFETs ON and OFF complimentary to each other regulates V_{OUT} to its set value.Observe that the low-side MOSFET will not turn ON automatically. This action needs additional MOSFET drive circuitry within the control IC to turn ON and OFF as needed.

Compare this to asynchronous topology where the polarity reversal across the inductor automatically forward biases the diode,completing the circuit. In both the asynchronous and synchronous topologies, the effective switch is the high-side MOSFET. It is the switch which dictates when to build up energy in the inductor and when to force the inductor current to start freewheeling.

In the synchronous topology the low-side MOSFET's lower resistance from drain to source (RDS_{ON}) helps reduce losses significantly and therefore optimizes the overall conversion efficiency.

3.3 Design and Simulation Result of Synchronous Buck Regulator

Specifications: Input Voltage V_{in} (dc) = Output of synchronous flyback converter = 9.5V,
Switching Frequency = 100 KHz,
Outputs Specifications: (6.3V, 3.3A).

Step1: Calculation of Inductance (L)

$T_s = 1/f_s$ =10 µs, $D = V_0/V_{in}$ = 66%, P_{out} = 20.79 Inductor will be chosen so that the current remains continuous if the DC output current stays above a specified minimum value. (Typically this is chosen to be around 10% of the rated load current, or $0.1*I_o$, where "I_o" is defined as the nominal output current.)

Therefore, $I_{0\,(min)} = 0.1I_0 = (I_2 - I_1) / 2$ i.e. $\Delta I = 0.2I_o$= 0.66 A

$$L = [5(V_{IN} - V_0)* V_0*T_S] / [V_{IN} * I_0] = 32.15\ \mu H. \quad (16)$$

Step2: Calculation of Output capacitor (C_0):

$$C_0 = [(1-D)*T_S^2*V_0] / [8 * L* \Delta V_0] = 13.22\ \mu F \quad (17)$$

Where ΔV_0 = Consider 1% of V_0.

Step3: Calculation of R_{load}:

$$R_{load} = V_0 / I_0 = 1.91\ \Omega. \quad (18)$$

Simulation circuit:

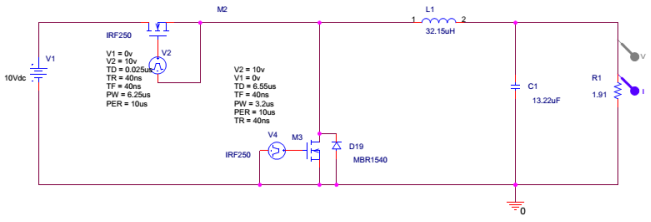


Fig -3.3: Schematic diagram of Synchronous buck converte

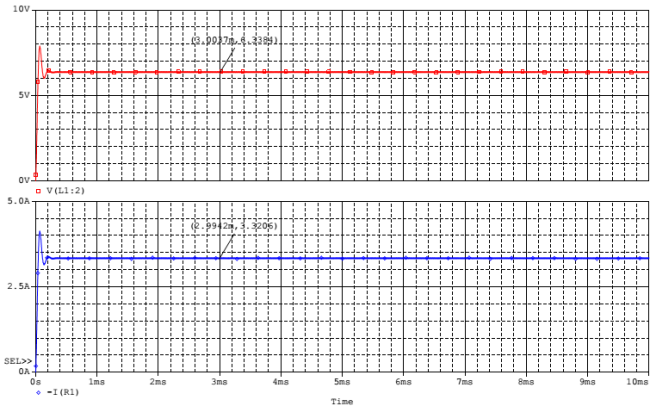


Fig -3.4: waveform of output voltage and output current of SR Buck converter.

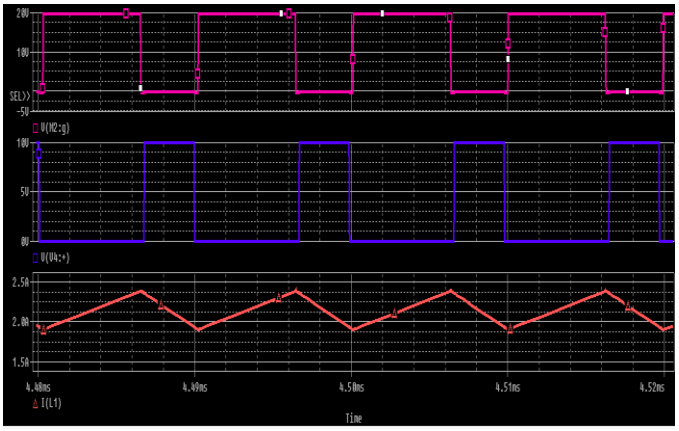


Fig -3.5: Waveform of gate pulse of mosfet M2 & M3 and Inductor current.

3.4 PWM Controller for Synchronous Buck Regulator

The LM5116 is a synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle by cycle current limiting and ease of loop compensation [8]. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications [8]. The operating frequency is programmable from 50 kHz to 1 MHz .The LM5116 drives external high-side and low-side NMOS power switches with adaptive dead time control [8].

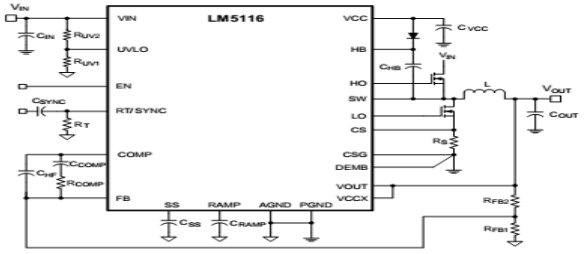


Fig -3.6: Typical application of LM5116[8].

4. PROPOSED TOPOLOGY OF SYNCHRONOUS FLYBACK CONVERTER WITH SYNCHR-ONOUS BUCK POST REGULATOR

In whole circuit, Secondary side of flyback converter will be floating on very high voltage line (i.e. 10kv or more).Therefore isolation is required between primary and secondary winding of flyback transformer. Also it is very difficult to take feedback signal for control circuit from secondary side of synchronous flyback converter to primary side, because voltage level of primary side is 28V DC whereas voltage level of secondary side of flyback converter is 10kv with respect to ground, as shown in fig. 4.1. So synchronous buck post regulator is implemented for obtaining regulated output of 6.3 V DC from 28 ± 0.5V DC input at 100 KHZ frequency.

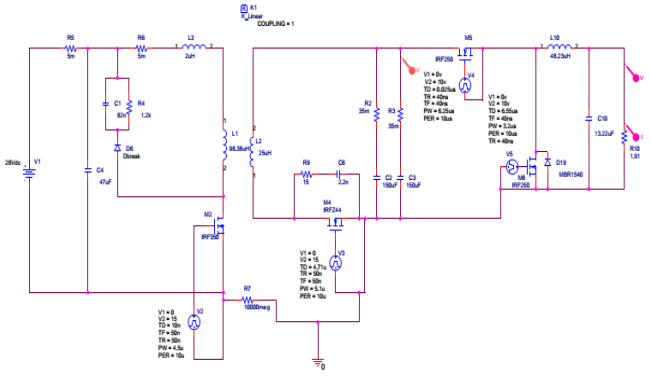


Fig -4.1: Schematic diagram of proposed circuit.

4.1 Simulation Result

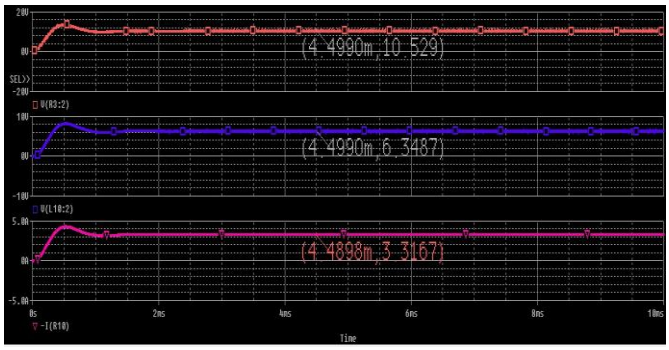


Fig -4.2: Waveform of input voltage of SR buck regulator and output voltage and output current of proposed topology.

5. HARDWARE IMPLEMENTATION OF PROPOSED TOPOLOGY AND TESTING RESULT

To implement the hardware as per proposed topology and design mentioned in sections 2.1, 2.2 and 3.3, cascaded circuit is used. In cascaded circuit, 1st stage is synchronous flyback converter and 2nd stage is synchronous buck regulator. Applied input is 28 ± 0.5V DC with 100 kHz switching frequency and regulated output of 6.6 V DC obtained by using IC UC28025 in primary side of flyback converter, IC FAN6204 in secondary side of flyback converter and IC LM 5116 in 2nd stage of cascaded circuit for regulation.

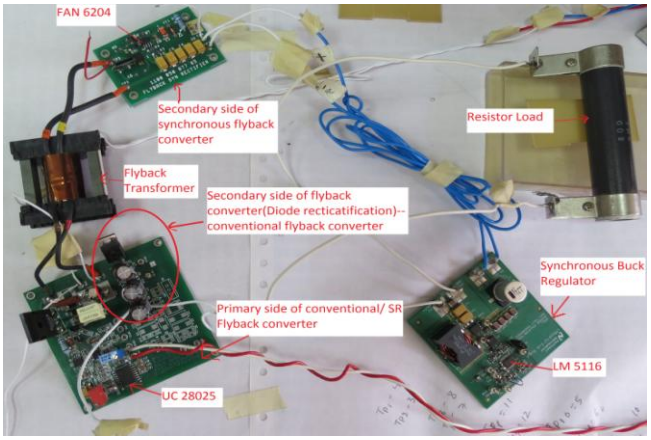


Fig -5.1: (a) Detailed hardware circuit

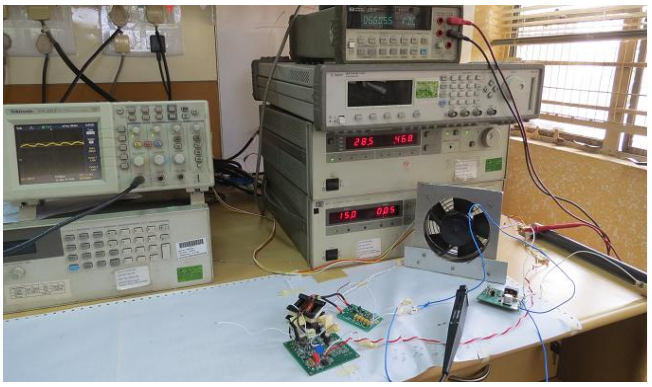


Fig -5.1: (b) Hardware circuit with output result at 3.9Ω Load.

5.1 Waveform of Hardware Circuit

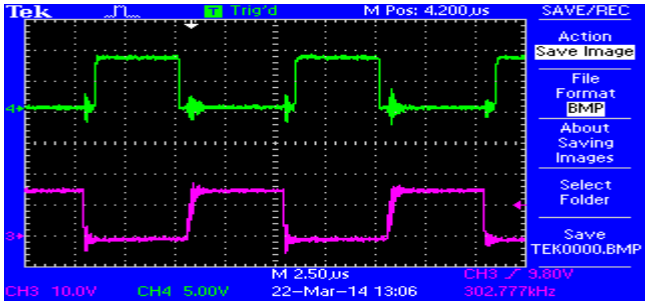


Fig -5.2: ch.3-prmary and ch.4 secondary gate pulse of synchronous flyback converter in proposed topology.

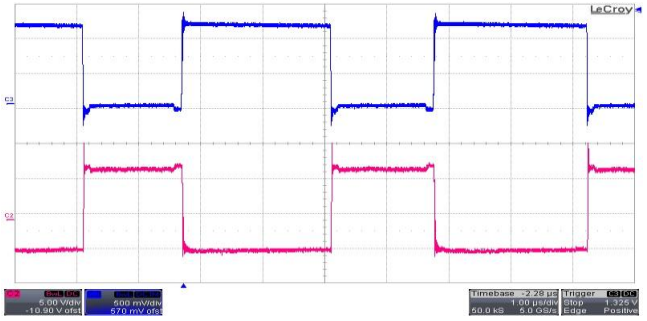


Fig -5.3:ch.3- primary and ch2. – Secondary mosfet voltage (V_{DS}) of sync. Buck regulator in proposed topology.

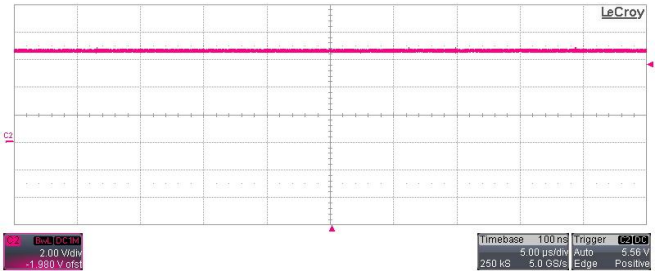
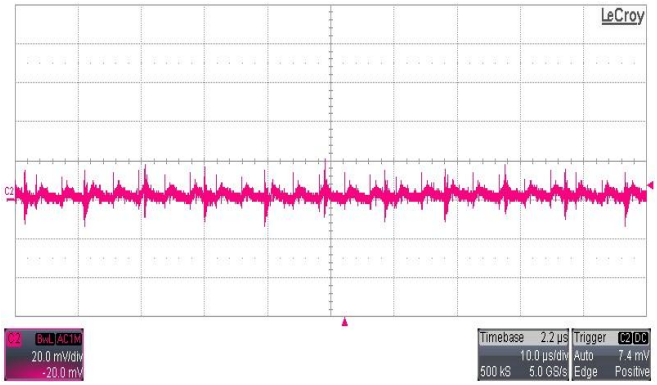
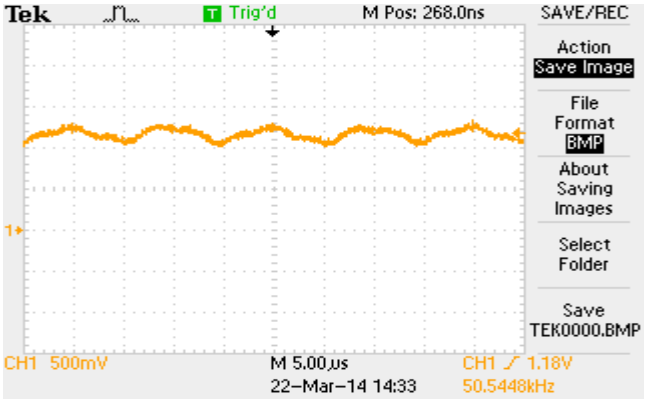


Fig -5.4: Regulated output voltage (6.6V) of proposed topology.



(a)



(b)

Fig -5.5: (a) Ripple voltage & (b) Ripple current of proposed Topology.

5.2 Testing Result of Hardware Circuit

Table -1: Simple (conventional) flyback converter (open loop)

At The $R_{load} = 5\Omega$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
27.5	0.727	19.99	9.39	1.84	17.28	86.42
28	0.740	20.72	9.57	1.87	17.9	86.37
28.5	0.757	21.57	9.76	1.91	18.64	86.41

Table -2: Synchronous flyback converter (open loop)

When $R_{load} = 5\ \Omega$ (Full load)

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
27.5	0.765	21.04	9.77	1.99	19.44	92.42
28	0.778	21.78	9.92	2.02	20.04	91.99
28.5	0.795	22.66	10.12	2.07	20.95	92.46

Table -3: Only Synchronous Buck Regulator (Closed loop)

When $R_{load} = 2\Omega$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
8.02	2.84	22.78	6.62	3.31	21.91	96.18
9.06	2.52	22.83	6.62	3.31	21.91	95.97
10.04	2.28	22.89	6.62	3.31	21.91	95.72
11.02	2.09	23.03	6.62	3.31	21.91	95.14
13.01	1.777	23.12	6.62	3.31	21.91	94.76

Table – 4: Synchronous Flyback Converter Cascaded with Synchronous Buck Regulator (Full Hardware Circuit)

When $R_{load} = 2\ \Omega$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
27.5	0.982	27.01	6.57	3.5	22.995	85.15
28	0.969	27.13	6.57	3.5	22.995	84.75
28.5	0.956	27.25	6.57	3.5	22.995	84.4

6. CONCLUSIONS

Design of synchronous Flyback Converter with synchronous Buck post regulator is proposed in this paper. This proposed topology has several outstanding characteristics. We achieved low voltage drop, less power losses & very high efficiency. It is suitable and simple to be used for power supplies with high-PWM frequency and low-output voltage to reduce the rectification loss. Since secondary side of this scheme is less dissipative, it is best suitable for heater converter stage of TWT Power supply floating on high voltage where cooling is an issue.

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