PERFORMANCE ANALYSIS OF CMOS COMPARATOR AND CNTFET COMPARATOR DESIGN

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Abstract

This paper presents an efficient, low power, fast-response Carbon NanoTube Field Effect Transistor (CNTFET) based comparator and shows the simulation results for the basic performance parameters for it. Due to the properties of Carbon Nanotube (CNT) the CNTFET devices show faster performance as compared to that of complementary metal oxide semiconductors (CMOS) devices. And hence CNTFET based comparator has to show much more improved performance compared to comparator design using CMOS. The performances such as delay, power and the transient results of the CNTFET comparator simulation are much more efficient. Both comparators are simulated in CADENCE.

Key Words: *Carbon Nano-Tube Field Effect Transistor (CNTFET), MOSFET, CADENCE, Comparator, Delay and Power.*

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1. INRTODUCTION

Silicon based MOS Technology is the basic cell of today's Very Large Scale Integrated systems. Moore's law predicts that CMOS Technology has continued to scale down which has now reached to 32nm and latest 22nm nano-meter range scale [2]. And it is difficult to go further since the controlling parameters will be the problem. For these small dimensions the systems has to suffer from many non-ideal effects like as lowered trans-conductance, source to drain tunnelling, gate oxide leakage, reduction in ON state current, mismatch in devices, fluctuations in doping patterns, degradation of mobility, delay problem etc. Such non-ideal effects results to increase in short channel which will rise exponentially, high power density and several variations in process. Again as we go further scaling down the fabrication process parameters are difficult to control and also overall processing cost increases for scaled devices.

According to the prediction of the Industrial Technology Roadmap (ITR), in nano-ranges the density on the chip will be very high and will encounter some difficulties in terms of technology limitations.

In the device operation phenomenon, Schottky Barrier (SB) is one of the CNTFETs (as shown in Fig-1(a) and as shown in Fig-1(b)). Good DC current can be achieved by SB-controlled and performances for low power and high speed can be limited. Thus we shall see the alternatives for silicon transistors [3]. With the unique properties and if we could fabricate precisely, the next nano transistor generation design can be CNT based elements, which is CNTFETs. Near around from the year 2015(as per prediction of ITR) silicon will be replaced by new materials and their devices. The CNTs are also recognised as "wonder material" of new century. These are also referred as the basic building blocks for silicon circuits [3]-[6]. CNTFET overcomes most of the basic limitations of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

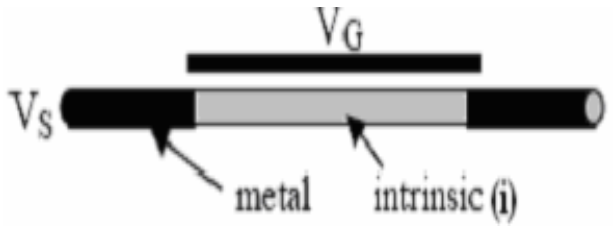

Fig -1(a): Schottky Barrier

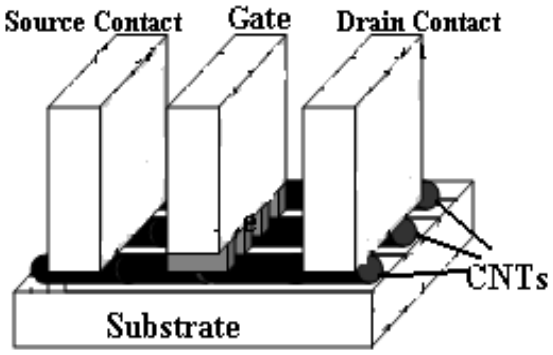

Fig -1(b): CNTFET

In this paper, section-2 describes the structure and characteristics of the device. Section-3 is presenting the design of classical comparator circuit and a new design. In section-4 performance parameters of CNTFET are compared with CMOS implementation. Finally section-5 concludes the paper.

2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Carbon Nanotubes (CNTs) are the allotropes of carbon having cylindrical nanostructure. Graphene sheets are rolled at specific and discrete angles called chiral angle. In 1991 Dr.Iijima has introduced multi-walled CNTs [9], and also the single walled CNT. The MWCNTs consists of two or more graphene sheets inside it. Depending on the chirality of the single walled CNTs, those can show its properties as metal or semiconductor. Single walled graphene sheet consists of one graphene cylinder and is rolled up with respect to a certain direction called chirality to form a nanotube. This direction is nothing but the tube axis represented as T [9], shown in Fig-2. on the graphene sheet, carbon atoms can be expressed as a function of integers (n,m). The chiral vector C which is perpendicular to the tube axis T, and is given by

$$\overline{C} = n\overline{a}_1 + m\overline{a}_2 \quad (1)$$

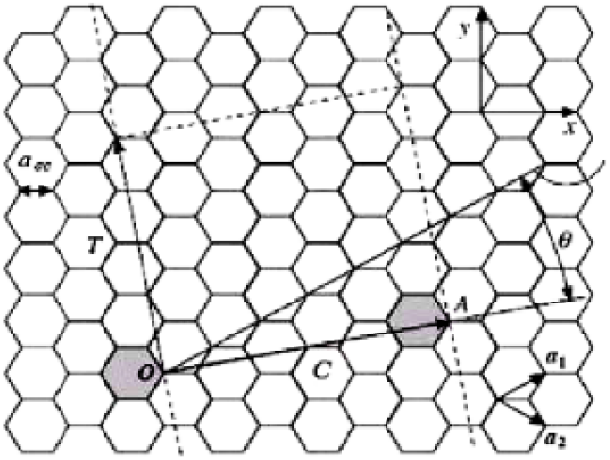

Fig -2: Graphene sheet and its parameters, i.,e, C-chiral vector, T-tube axis and θ-chiral angle

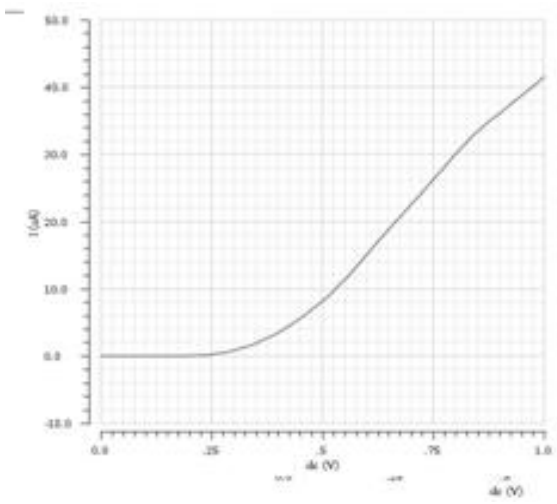

Fig -3: I-V Characteristics of CNTFET

The vector C decides, if the SWCNT is armchair or metallic, i.e. if n=m or n-m=3i, where i is an integer, it is armchair or metallic, if n = 0 or m = 0 the structure will be zigzag or chiral for other n and m values. The diameter of the SWCNT is

$$D_{CNT} = \frac{\overline{C}}{\pi} = \frac{a_{cc}\sqrt{3(m^2 + n^2 + mn)}}{\pi} \quad (2)$$

SWCNTs are the reason for the conduction channel in CNTFETs. Under gate between drain and source CNT shows as a channel region as in CMOS. The diameter of CNT is predefined during the generation process, the CNT width cannot be changed but depending on the number of CNTs used in width decides the current limit. CNTFETs have properties similar to MOSFETs but the manufacturing process of CNTFETs is simple as compared to CMOS which makes it as an almost ideal substitute to the MOSFET.

The operation of CNTFET and CMOS if compared they show almost same characteristics. But the CNTFET shows better current properties compared to CMOS, which is due to the heavy doping of source and drain. The gate barrier is useful for the controlling of electron flow through it, this barrier will generate the electric field and then allow electrons to flow through it after application of gate voltage.

Fig-3 shows I–V characteristics the CNTFET which are similar as MOSFET. The CNT channel has a threshold voltage which is the deciding factor for CNTFET and is given as: [11]

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{cnt}} \quad (3)$$

Where, a=2.49A^o is the carbon-to-carbon atom distance, V_π=3.033eV is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and DCNT is the CNT diameter.

3. COMPARATOR DESIGN

The comparator circuit is nothing but a circuit which compares an analog signal with another signal, another signal can be either analog signal or a reference signal and produces a output signal which is a binary signal. The comparator has two inputs and one output, and is divided into two basic stages [13].The first stage is the differential stage which after comparing two input signals give a current which is proportional to the input difference of voltages. The second stage is generating output logic depending on threshold voltages of the N and P CNTFET. Fig-4 shows the comparator circuit.
The total propagation delay is given as,

$$\Delta t = \Delta t_1 + \Delta t_2 \quad (4)$$

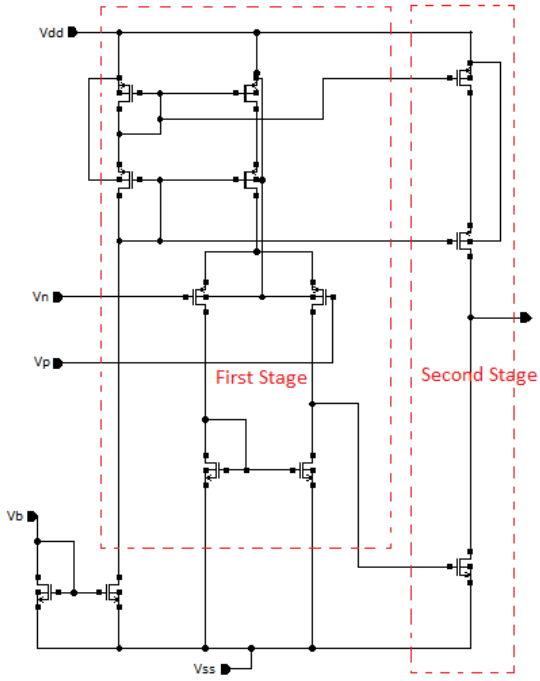

Fig -4: Classical comparator implementation with PMOS input stage[1]

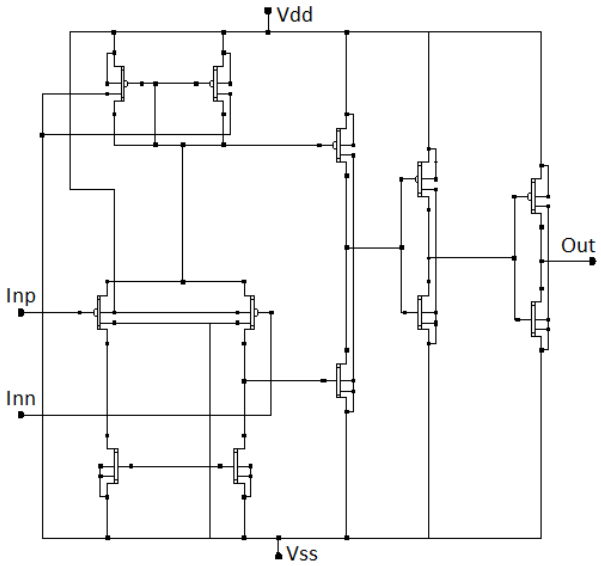

Fig -5: Circuit Design of efficient Comparator using CNTFET

4. RESULT ANALYSIS AND SIMULATION

The CNTFET comparator when properly biased. Through Inn and Inp two input signals are connected, i.e. one sinusoidal wave and another reference sig+nal. The transient results obtained are shown in Fig-6 (a), and for classical CMOS design the transient simulation is shown in Fig-6 (b).

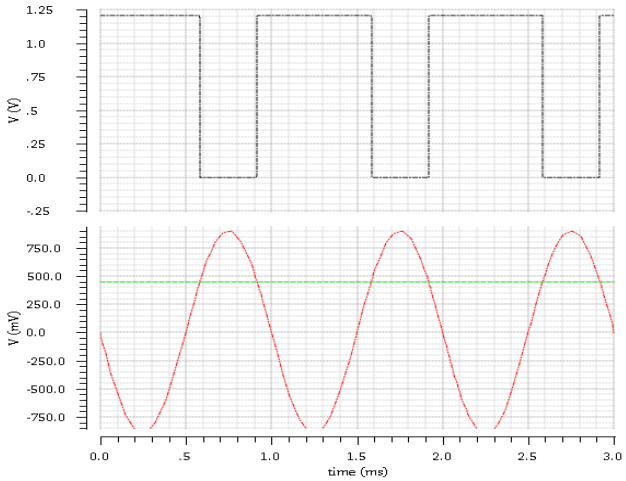

Fig -6(a): Transient Analysis of CNTFET Comparator Design

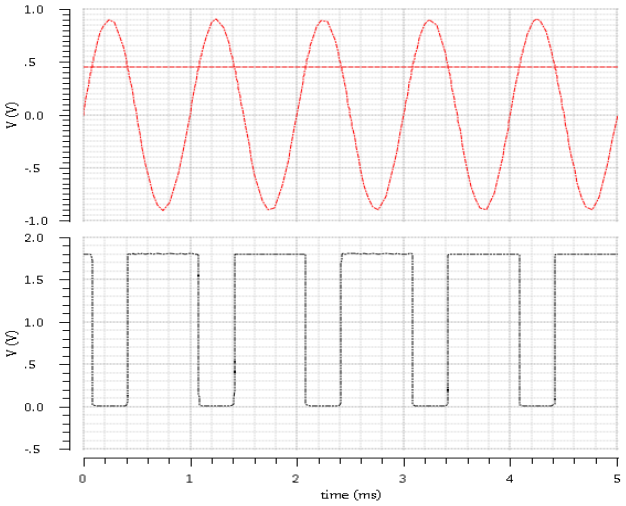

Fig -6(b): Transient Analysis of classical MOSFET Comparator Design

When the reference is 1V and another signal is varied from 0.9V to 1V and at proper biased condition, the magnified waveform to see the delay at nanoseconds range, is shown in Fig-7 (a) which shows results of classical CMOS comparator while Fig-7 (b) shows the results of CNTFET comparator design.

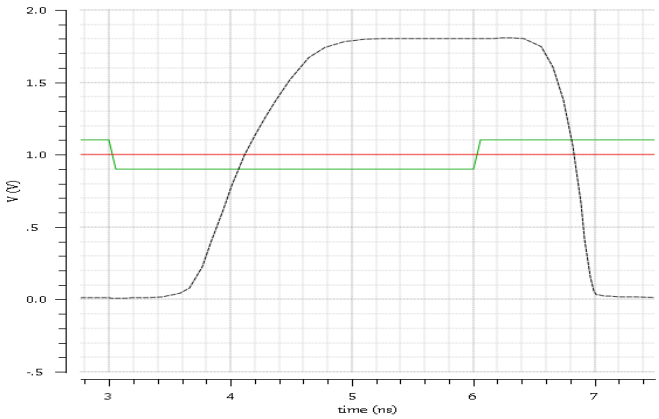

Fig -7(a): Rise and fall time analysis of classical Comparator

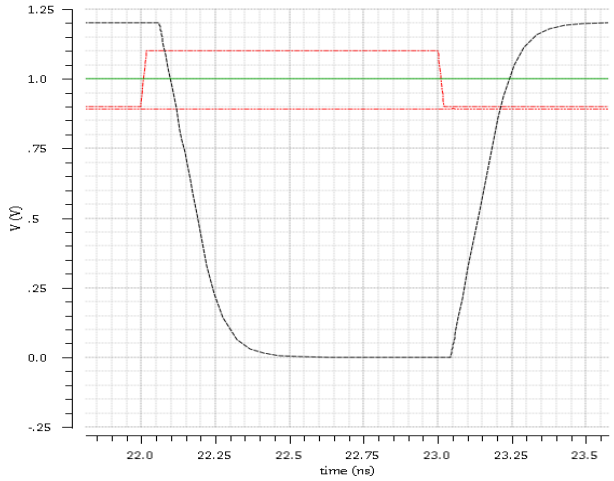

Fig -7(b): Rise and fall time analysis of CNTFET Comparator

When the time delay for rise and fall events are calculated the result has shown that CNTFET comparator device gives much more faster results than that of classical CMOS comparator. The rise time for the classical comparator is 1.03ns, and for CNTFET comparator is 142.1µs. And fall time for classical and CNTFET comparators are 821.476µs and 164.18µs, respectively and such results are advantageous due to capacitance between gate capacitance and drain source capacitance of CNTFET.

Table given below shows the summary of simulation results:

Performance parameters	comparators	
	CMOS	**CNTFET**
Rise delay	0.961ns	0.142ns
Fall delay	0.8215ns	0.1642ns
Average power	910mW	118mW

Table -1: Comparison between MOSFET and CNTFET comparators

3. CONCLUSIONS

This paper compares the classical CMOS and CNTFET comparator design for performances like rise time, fall time delay, average power consumption and transient analysis. These comparators are simulated in CADENCE tool with 32nm technology for CNTFET and 180nm technology for CMOS devices as given in Table1. From summary of table, it can be concluded that the CNTFET comparator shows quiet good performance like faster output response, less average dissipation of power, and improved transient response. Due to the promising feature of carbon-based devices the possibility of replacing silicon device with carbon devices cannot be neglected.

REFERENCES

[1] Syed Mustafa Khelat Bari, Nur-e-elahi Shonchoy, Farah Tasnuba Kabir, Arif Khan, "Design and Performance Analysis of Ultra Fast CNTFET Comparator and CMOS Implementation Comparison" 14th International Conference on Modelling and Simulation- 2012.

[2] "A Semiconductor Industry Association International Technology Roadmap for Semiconductors—2008" Update: Overview and Summaries, 2008. http://www.itrs.net/Links/2008ITRS/Home2008.hm.

[3] Ref H.-S. P. Wong, "Beyond the conventional transistor", Solid- State Electronics, vol. 49, issue 5, pp. 755-762, 2004. Refere Tans, S. A. Verschaerea and C. Dekker, "Room temperature transistor based on a SWCN," Science, 397: 49-52, 1998.

[4] S.Heinze, J. Tersoff, R. Martel, V. Derycke, J.Appenzeller, and P.Avouris, "Carbon nanotubes as Schottky barrier transistors," Phys. Rev.Lett., vol. 89, no. 10, pp. 106 801-1–106801-4, 2002.

[5] Refer Y. Lin, J. Appenzeller, J. Knoch, P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," IEEE Trans. Nanotechnol.,Vol 4, Issue 5, pp 481 - 489, Sept. 2005.

[6] Peng, N., H. Li and Q. Zhang, 2009. "Nano Scale contacts between carbon Nanotubes and metallic Pads," Acsnano, 10: 1016-25. 11.

[7] J. Deng and H.-S P. Wong, ―A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part I: Model of the Intrinsic Channel Region, Submitted to IEEE Transactions on Electron Devices, 2007.

[8] S. Iijima,, "Helical microtubules of graphitic carbon", Nature, 354, 56-8, 1991.

[9] Stanford University CNTFET Model Website. (2008). [Online]. Available: http://nano.stanford.edu/ model.php?id=23

[10] J. Appenzeller, "Carbon nanotubes for high-performance electronics Progress and prospect", Proc. IEEE, vol. 96, no. 2, pp. 201–211, Feb.2008.

[11] J. Guo and M. Lundstrom―"Role of Phonon Scattering In Carbon Nanotube Field-Effect Transistors", Applied Physics Letters, vol. 86,pp. 193103, 2005.

[12] P. E. Allen and D. R. Holberg, 2002, "CMOS Analog Circuit Design", 2nd Edition, Oxford. University Press, 2002.

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